
Upgrading to the TVP5146M2

Mixed Signal Video Group

ABSTRACT

TVP5146M2 ROM (08.00) Comparison

In this document, only those additional features that are pertinent to TVP5146M2 are described. For more information, see the TVP5146M2 data sheet, TI literature number [SLES141](#). Date: August 2005

1 Functional Improvements

The M2 suffix within the TVP5146M2 part number indicates a firmware upgrade to the baseline TVP5146. Improvements within this upgrade are:

- Eliminate the need to use previous RAM codes
- Improved weak signal performance
 - Improved PLL stability and AGC control help to have better weak signal performance on even lower signal quality.
- Improved AGC performance
 - Added AGC decrement speed control
 - Added AGC decrement delay
 - New color AGC algorithm
 - Added the extended AGC range control
 - Additional back-end AGC control by providing conditional enable
- Improved VCR trick mode performance
 - Improved algorithms help adapt better to different number of lines per frame and different number of pixels per line.
 - Some video signals have longer line length at the beginning of the frame, causing image instability.
- Better adaptability to nonstandard signals
 - Higher stability in PLLs helps the video decoder adapt and synchronize to video signals with nonstandard number of lines per frame or pixels per line.
- Improved horizontal and vertical image stability and faster lock speeds, including color lock
 - Improved internal PLL control algorithm speeds on converging to references of PLLs
- Improved SECAM performance
 - Modified SECAM color noise by improved controlling of the filters
 - Color anomaly at top of screen resolution is an outcome of improved filter control.
- I²C register and pin compatible to TVP5146
- No need to pull down C1 (pin 69) with a 2.2-k Ω resistor
- Improved auto-switch performance
 - Improved lock ability to low color burst amplitudes speeds up the auto switch.
 - Even when there is no color burst, the chip continues to match the modes that have same number of lines as it was before losing color burst.

2 Power-On Sequence

In the TVP5146, the user is required to use the register settings in [Table 1](#) after reset is applied.

Note: For TVP5146M2, the below settings are not necessary and must not be written, except step 10 and step 11.

Table 1. Power-On Register Settings for TVP5146

STEP	REGISTER	DATA
1	0xE8	0x02
2	0xE9	0x00
3	0xEA	0x80
4	0xE0	0x01
5	0xE8	0x60
6	0xE9	0x00
7	0xEA	0xB0
8	0xE0	0x01
9	0xE0	0x00
10	0x03	0x01
11	0x03	0x00

3 Firmware Improvements

There have been changes in the ROM code of the TVP5146M2 with respect to TVP5146. Also this firmware upgrade eliminates the need to load previous TVP5146 RAM codes.

Note: Previous RAM codes do not work with TVP5146M2 and must not be loaded.

3.1 AGC Block Algorithm

The AGC block in the TVP5146M2 has an improved algorithm for controlling the gain value with respect to the input source amplitude and fluctuations. This is achieved by controlling the increment and decrement gains and speeds on composite inputs. The registers for this feature are shown in the following table:

REGISTER DESCRIPTION	REGISTER SUBADDRESS	DEFAULT VALUE	BITS AND LOCATION
AGC increment speed	78h	05h	2:0
AGC increment delay	79h	1Eh	7:0
AGC decrement speed ⁽¹⁾	6Fh	04h	2:0
AGC decrement delay	9Eh	00h	7:0

⁽¹⁾ For composite/luma peaks only

3.2 AGC Range Control

The TVP5146M2 has an added feature for AGC range selection. There are three possible ranges of AGC gains selectable by this register. These ranges are selected according to the signal source fluctuations.

REGISTER DESCRIPTION	REGISTER SUBADDRESS	DEFAULT VALUE	BITS AND LOCATION
AGC range control	9Fh	06h	2:0

Gain ranges selectable are:

101	1.25 – 1.0
110	1.5 – 1.0 (default)
111	1.75 – 1.0

Other choices of these three bits are reserved.

3.3 Color AGC Threshold Control

The TVP5146M2 adds a register for controlling the color AGC threshold. The color AGC is activated when the chroma amplitude reaches the threshold set in bits 3:0 of this register.

REGISTER DESCRIPTION	REGISTER SUBADDRESS	DEFAULT VALUE	BITS AND LOCATION
CAGC control	6Ah	0Ah	4:0

To enable this control, bit 4 must be set to 1.

3.4 Back-End AGC Control

In the TVP5146M2, the following register allows the back-end AGC to be disabled when the front-end AGC uses specific references as described below.

REGISTER DESCRIPTION	REGISTER SUBADDRESS	DEFAULT VALUE	BITS AND LOCATION
Back-end AGC control	6Ch	08h	2:0

D0 = 1 is used to disable back-end AGC when front-end AGC uses sync height for the reference. Default is 0.

D1 = 1 is used to disable back-end AGC when front-end AGC uses color burst for the reference. Default is 0.

D2 = 1 is used to disable back-end AGC when front-end AGC uses composite peak for the reference. Default is 0.

D3 must always be from fifth set to 1.

3.5 F-Bit and V-Bit Control

Register 0x69 and 0x75 control F-bit and V-bit decode and control methods with the ITU-656 data output. When using ITU-656, use of these registers may be adjusted in order to improve the VCR trick mode and nonstandard video performance. For more information, see the TVP5146M2 data sheet, TI literature number [SLES141](#).

3.6 ROM Version

ROM version of the TVP5146M2 can be read from register 0x70. This is a read-only register and the value is 0x08 for TVP5146M2.

REGISTER DESCRIPTION	REGISTER SUBADDRESS	DEFAULT VALUE	BITS AND LOCATION
ROM version	70h	0x08h	7:0

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