



TPS791

超低ノイズ、高PSRR、高速RF 100mA低ドロップアウト・リニア・レギュレータ

1 特長

- EN付きの100mA低ドロップアウト・レギュレータ
- 1.8V、3.3V、4.7V、および可変出力電圧製品
- 高PSRR (10kHz時70dB)
- 超低ノイズ(15 μ V_{RMS})
- 高速起動時間(63 μ s)
- 1 μ Fのセラミック・コンデンサで安定動作
- 優れた負荷/ライン過渡応答
- 超低ドロップアウト電圧(全負荷時38mV、TPS79147)
- 5ピンSOT23 (DBV)パッケージ
- TPS792xxはENオプション付き

2 アプリケーション

- VCOおよびPLL駆動
- Bluetoothおよび無線LAN
- 携帯機器およびバッテリー駆動機器

3 概要

TPS791は、低ドロップアウト(LDO)/低消費電力のリニア電圧レギュレータであり、電源リップル除去比(PSRR)が高く、超低ノイズ、高速起動、優れたライン/負荷過渡応答を小型のSOT23パッケージで実現しています。出力への小型の1 μ Fセラミック・コンデンサで安定して動作します。

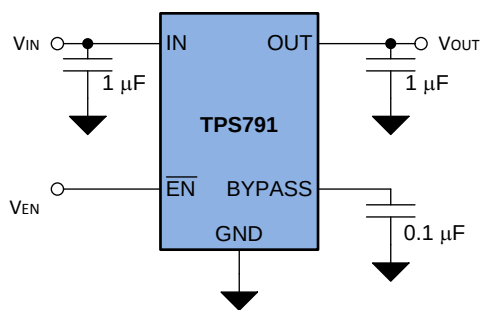
TPS791は高度な独自のBiCMOSプロセスを採用して、極めて低いドロップアウト電圧を実現しています(TPS79147で100mA時38mVなど)。高速起動(0.001 μ Fのバイパス・コンデンサを使用した場合に約63 μ s)を達成しながら、静止電流は極めて低く抑えることができます(標準値170 μ A)。加えて、スタンバイ・モードでは消費電流が1 μ A未満まで抑えられます。0.1 μ Fのバイパス・コンデンサを使用することで、TPS79118の出力電圧ノイズは約15 μ V_{RMS}となります。高PSRR、低ノイズ、高速応答といった特性は、携帯型のRF電子機器などノイズに敏感なアナログ回路のアプリケーションに最適です。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS791	SOT23 (5)	2.90mm×1.60mm
	SOT23 (6)	2.90mm×1.60mm

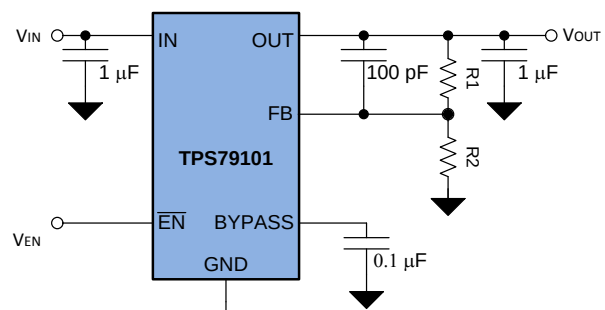
(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図: 固定出力



Copyright © 2018, Texas Instruments Incorporated

概略回路図: 可変出力



Copyright © 2017, Texas Instruments Incorporated



目次

1	特長	1	7.4	Device Functional Modes.....	15
2	アプリケーション	1	8	Application and Implementation	16
3	概要	1	8.1	Application Information.....	16
4	改訂履歴	2	8.2	Typical Application	16
5	Pin Configuration and Functions	3	8.3	Do's and Don'ts.....	17
6	Specifications	3	9	Power Supply Recommendations	18
6.1	Absolute Maximum Ratings	3	10	Layout	18
6.2	ESD Ratings.....	4	10.1	Layout Guidelines	18
6.3	Recommended Operating Conditions.....	4	10.2	Layout Example	18
6.4	Thermal Information	4	11	デバイスおよびドキュメントのサポート	19
6.5	Electrical Characteristics.....	5	11.1	ドキュメントの更新通知を受け取る方法.....	19
6.6	Typical Characteristics.....	6	11.2	コミュニティ・リソース	19
7	Detailed Description	12	11.3	商標	19
7.1	Overview	12	11.4	静電気放電に関する注意事項	19
7.2	Functional Block Diagrams	12	11.5	Glossary	19
7.3	Feature Description.....	13	12	メカニカル、パッケージ、および注文情報	19

4 改訂履歴

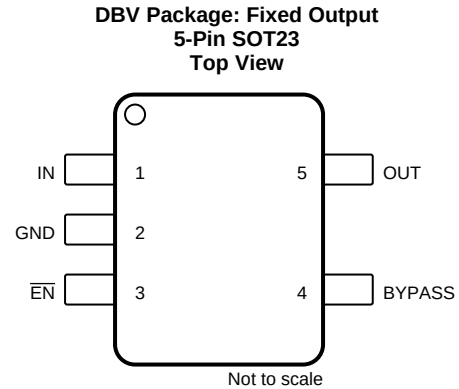
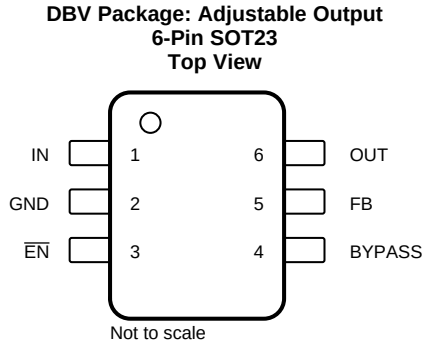
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (May 2002) から Revision D に変更

Page

• 「製品情報」の表、「概略回路図」の図(p.1)、「ESD 定格」の表、「熱に関する情報」の表、「ピン構成および機能」セクション、「概要」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• ドキュメント全体でTPS791xxをTPS791に変更.....	1
• 「アプリケーション」セクション 変更	1
• 「概要」セクション 変更	1
• Deleted <i>Ordering Information</i> table	3
• Changed $\overline{\text{EN}}$ pin description	3
• Added I/O data for GND pin	3
• Deleted <i>Package Dissipation Rating</i> table	3
• Changed V_I to V_{IN} , I_O to I_{OUT} , C_O to C_{OUT} , $C_{O(byp)}$ and $C_{(byp)}$ to C_{BYPASS} throughout document	3
• Changed formula in footnote 1 of <i>Recommended Operating Conditions</i> table.....	4
• Added VREF parameter to <i>Electrical Characteristics</i> table.....	5
• Changed V_{CC} to V_{IN} in test conditions of <i>UVLO threshold</i> and <i>UVLO hysteresis</i> parameters.....	5
• Added PSRR and V_{DO} symbols to <i>Power-supply ripple rejection</i> and <i>Dropout voltage</i> parameters.....	5
• Added conditions statement to <i>Typical Characteristics</i> section	6
• Changed I_{OUT} to C_{BYPASS} in <i>TPS79118 Output Spectral Noise Density vs Frequency</i> figure	7
• Changed I_{OUT} to C_{BYPASS} in <i>TPS79133 Output Spectral Noise Density vs Frequency</i> figure	7
• Changed third bullet in <i>Normal Operation</i> section	15
• Changed first bullet in <i>Disabled</i> section	15
• Changed V_{EN} column in <i>Device Functional Mode Comparison</i> table.....	15
• Added active-low to <i>Application Information</i> description	16

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	ADJ	FIXED		
BYPASS	4	4	—	An external bypass capacitor connected to this pin, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
$\overline{\text{EN}}$	3	3	I	The $\overline{\text{EN}}$ pin is an input which enables or shuts down the device. The enable signal is an active-low digital control that enables the device, so when $\overline{\text{EN}}$ is a logic high ($> 2 \text{ V}$), the device is in shutdown mode. When $\overline{\text{EN}}$ is logic low ($< 0.7 \text{ V}$), the device is enabled.
FB	5	N/A	I	This pin is the feedback input voltage for the adjustable device.
GND	2	2	—	Regulator ground.
IN	1	1	I	The IN pin is the input to the device.
OUT	6	5	O	The OUT pin is the regulated output of the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input voltage range ⁽²⁾	−0.3	6	V
Voltage range at $\overline{\text{EN}}$	−0.3	$V_{\text{IN}} + 0.3$	V
Voltage on OUT	−0.3	6	V
Peak output current	Internally limited		
Continuous total power dissipation	See Thermal Information table		
Operating virtual junction temperature, T_J	−40	150	°C
Operating ambient temperature, T_A	−40	85	°C
Storage temperature, T_{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground pin.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD} Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN} Input voltage ⁽¹⁾	2.7		5.5	V
I_{OUT} Continuous output current ⁽²⁾	0		100	mA
T_{J} Operating junction temperature	–40		125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_{\text{IN(min)}} = V_{\text{OUT(max)}} + \text{dropout voltage } (V_{\text{DO}}) \text{ at maximum load.}$$

(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but the device is not recommended to be operated under conditions beyond those specified in this table for extended periods of time.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS791		UNIT
		DBV (SOT23)	DBV (SOT23)	
		5 PINS	6 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	192.6	168.2	°C/W
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	104.2	87.1	°C/W
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	55.2	36.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.1	17.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.8	36.6	°C/W
$R_{\theta\text{JC(bot)}}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, ($T_J = -40^{\circ}\text{C}$ to 125°C), $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $\overline{\text{EN}} = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	TPS79101	T _J = 25°C, 1.22 V ≤ V _{OUT} ≤ 5.2 V		V _{OUT}			V
		0 μA < I _{OUT} < 100 mA ⁽¹⁾ , 1.22 V ≤ V _{OUT} ≤ 5.2 V		0.98 V _{OUT}	1.02 V _{OUT}		
	TPS79118	T _J = 25°C		1.8			
		0 μA < I _{OUT} < 100 mA, 2.8 V < V _{IN} < 5.5 V		1.764	1.836		
	TPS79133	T _J = 25°C		3.3			
		0 μA < I _{OUT} < 100 mA, 4.3 V < V _{IN} < 5.5 V		3.234	3.366		
	TPS79147	T _J = 25°C		4.7			
		0 μA < I _{OUT} < 100 mA, 5.2 V < V _{IN} < 5.5 V		4.606	4.794		
VREF	Reference voltage				1.2246		V
Quiescent current (GND current)		0 μA < I _{OUT} < 100 mA, T _J = 25°C		170			μA
		0 μA < I _{OUT} < 100 mA		250			
Load regulation		0 μA < I _{OUT} < 100 mA, T _J = 25°C		5			mV
ΔV _{OUT} /V _{OUT}	Output voltage line regulation ⁽²⁾		V _{OUT} + 1 V < V _{IN} ≤ 5.5 V, T _J = 25°C		0.05		% / V
			V _{OUT} + 1 V < V _{IN} ≤ 5.5 V		0.12		
Output noise voltage (TPS79118)		BW = 100 Hz to 100 kHz, I _{OUT} = 100 mA, T _J = 25°C	C _{BYPASS} = 0.001 μF	32		μV _{RMS}	
			C _{BYPASS} = 0.0047 μF	17			
			C _{BYPASS} = 0.01 μF	16			
			C _{BYPASS} = 0.1 μF	15			
Time, start-up (TPS79133)		R _L = 33 Ω, C _{OUT} = 1 μF, T _J = 25°C	C _{BYPASS} = 0.001 μF	53		μs	
			C _{BYPASS} = 0.0047 μF	67			
			C _{BYPASS} = 0.01 μF	98			
Output current limit		V _{OUT} = 0 V ⁽¹⁾		285	600	mA	
UVLO threshold		V _{IN} rising		2.25	2.65	V	
UVLO hysteresis		T _J = 25°C, V _{IN} rising		100		mV	
Standby current		$\overline{\text{EN}}$ = V _{IN} , 2.7 V < V _{IN} < 5.5 V		0.07	1	μA	
High level enable input voltage		2.7 V < V _{IN} < 5.5 V		2		V	
Low level enable input voltage		2.7 V < V _{IN} < 5.5 V			0.7	V	
Input current ($\overline{\text{EN}}$)		$\overline{\text{EN}}$ = V _{IN}		−1	1	μA	
PSRR	Power-supply ripple rejection	TPS79118	f = 100 Hz, T _J = 25°C, I _{OUT} = 10 mA	80		dB	
			f = 100 Hz, T _J = 25°C, I _{OUT} = 100 mA	75			
			f = 10 kHz, T _J = 25°C, I _{OUT} = 100 mA	72			
			f = 100 kHz, T _J = 25°C, I _{OUT} = 100 mA	45			
	TPS79133	f = 100 Hz, T _J = 25°C, I _{OUT} = 10 mA	70				
		f = 100 Hz, T _J = 25°C, I _{OUT} = 100 mA	75				
		f = 10 kHz, T _J = 25°C, I _{OUT} = 100 mA	73				
		f = 100 kHz, T _J = 25°C, I _{OUT} = 100 mA	37				
V _{DO}	Dropout voltage ⁽³⁾	TPS79133	I _{OUT} = 100 mA, T _J = 25°C	50		mV	
			I _{OUT} = 100 mA	90			
	TPS79147	I _{OUT} = 100 mA, T _J = 25°C	38				
		I _{OUT} = 100 mA	70				

(1) The minimum V_{IN} operating voltage is 2.7 V or $V_{OUT(\text{typ})} + 1\text{ V}$, whichever is greater. The maximum V_{IN} voltage is 5.5 V . The maximum output current is 100 mA .

(2) If $V_{OUT} \leq 1.8\text{ V}$ then $V_{IN\text{min}} = 2.7\text{ V}$ and $V_{IN\text{max}} = 5.5\text{ V}$.

(3) Equals V_{IN} voltage – $V_{OUT(\text{typ})} - 100\text{ mV}$; the TPS79118 dropout voltage is limited by the minimum input voltage range limitations.

6.6 Typical Characteristics

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

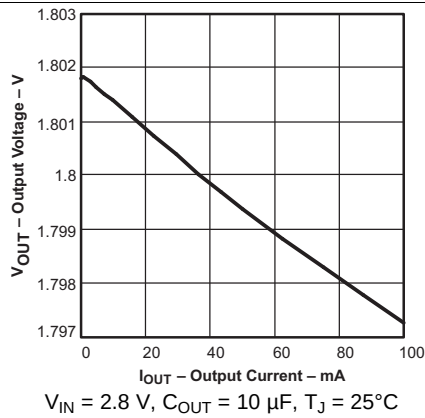


Figure 1. TPS79118 Output Voltage vs Output Current

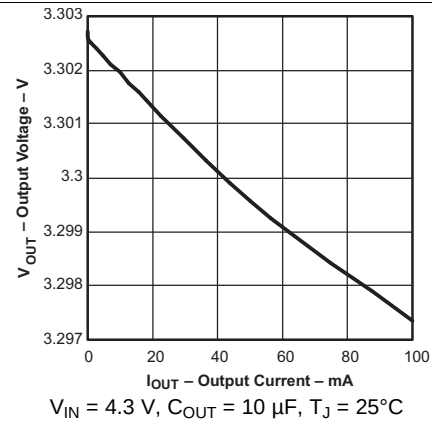


Figure 2. TPS79133 Output Voltage vs Output Current

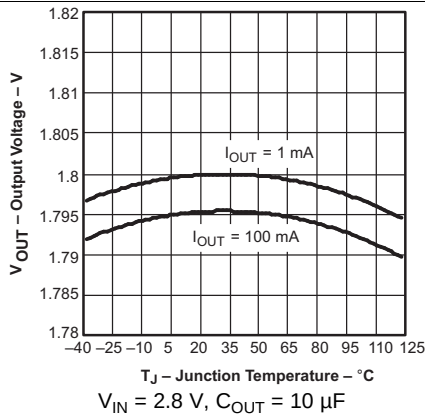


Figure 3. TPS79118 Output Voltage vs Junction Temperature

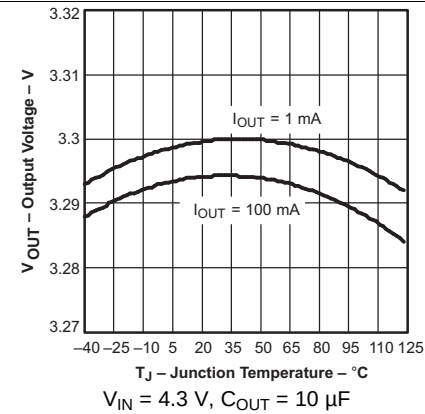


Figure 4. TPS79133 Output Voltage vs Junction Temperature

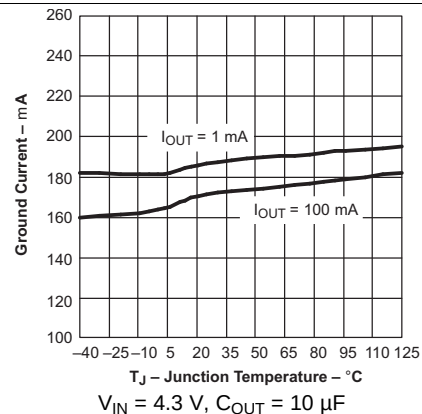


Figure 5. TPS79133 Ground Current vs Junction Temperature

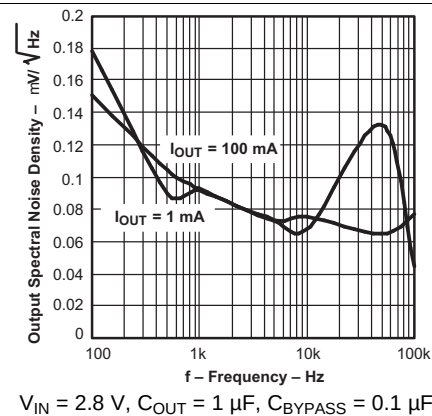
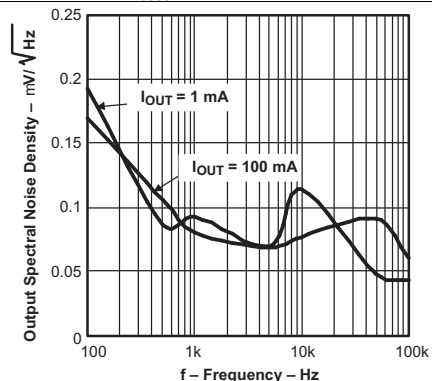


Figure 6. TPS79118 Output Spectral Noise Density vs Frequency

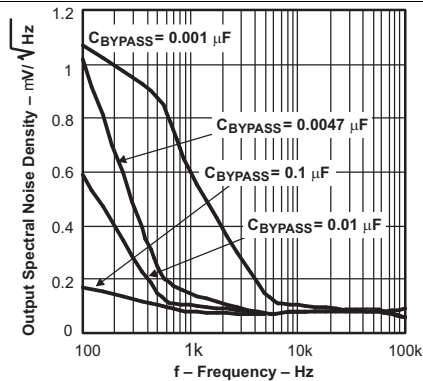
Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)



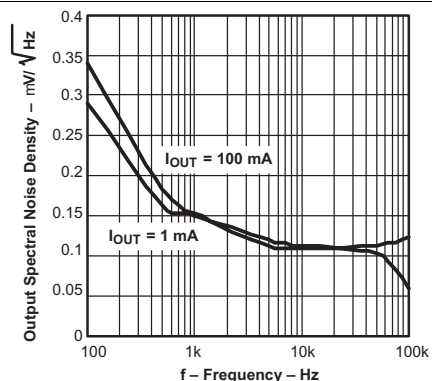
$V_{IN} = 2.8\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 7. TPS79118 Output Spectral Noise Density vs Frequency



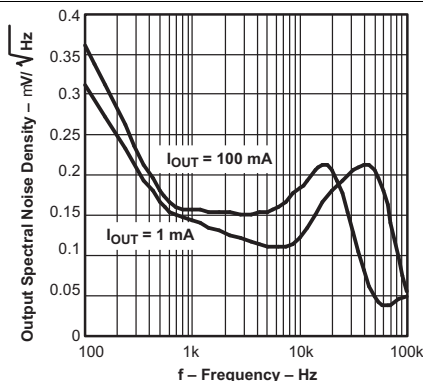
$V_{IN} = 2.8\text{ V}$, $I_{OUT} = 100\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 8. TPS79118 Output Spectral Noise Density vs Frequency



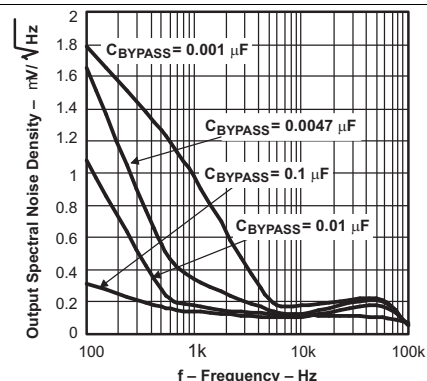
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 9. TPS79133 Output Spectral Noise Density vs Frequency



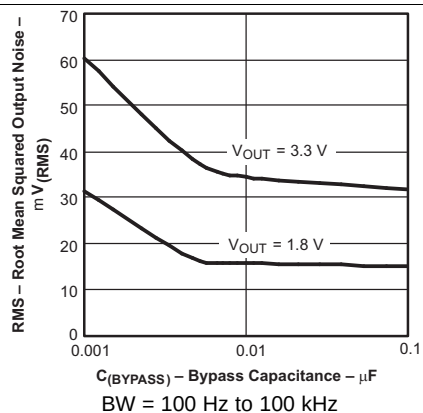
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 10. TPS79133 Output Spectral Noise Density vs Frequency



$V_{IN} = 4.3\text{ V}$, $I_{OUT} = 100\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$

Figure 11. TPS79133 Output Spectral Noise Density vs Frequency



$BW = 100\text{ Hz to }100\text{ kHz}$

Figure 12. Root Mean Squared Output Noise vs Bypass Capacitance

Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

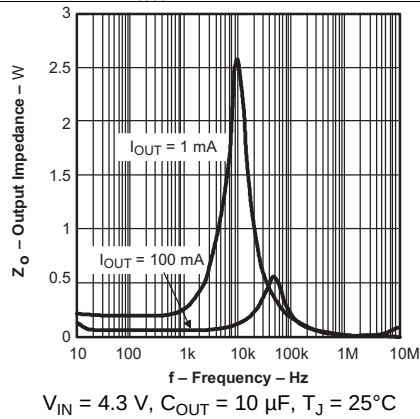


Figure 13. TPS79133 Output Impedance vs Frequency

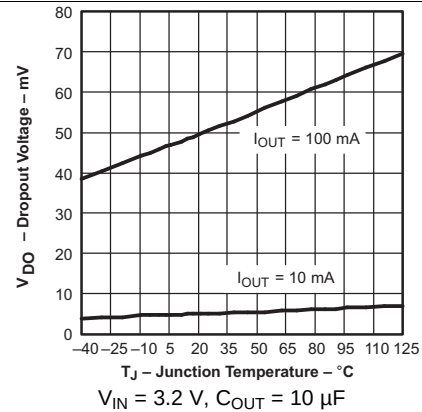


Figure 14. TPS79133 Dropout Voltage vs Junction Temperature

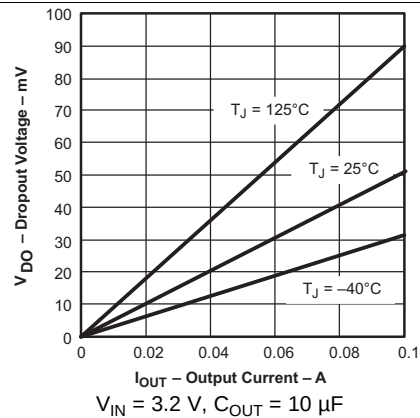


Figure 15. TPS79133 Dropout Voltage vs Output Current

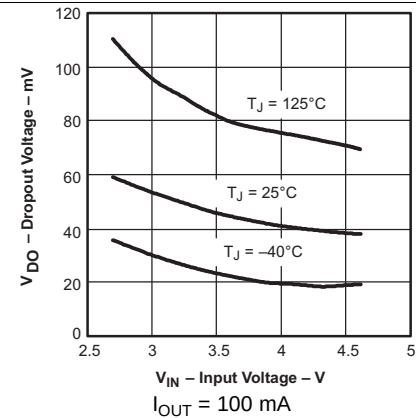


Figure 16. TPS79101 Dropout Voltage vs Input Voltage

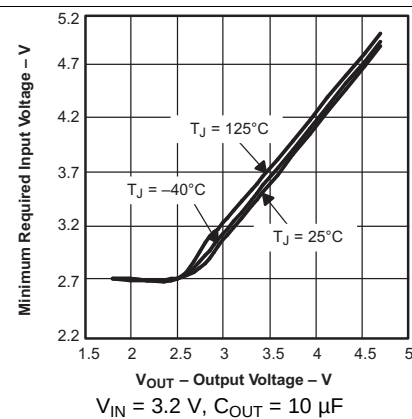


Figure 17. Minimum Required Input Voltage vs Output Voltage

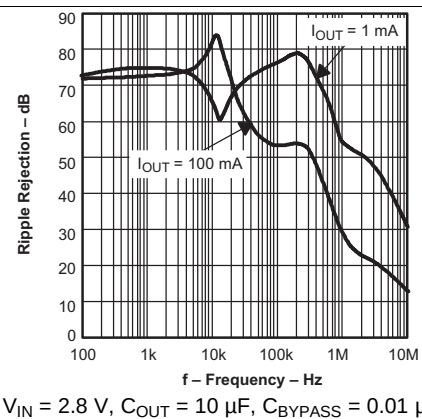
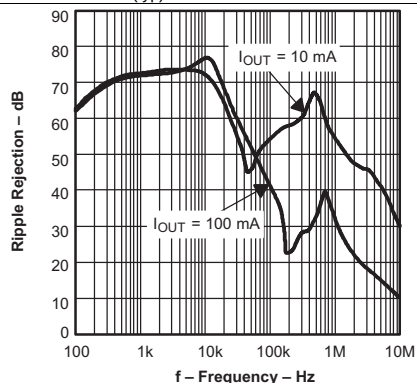


Figure 18. TPS79118 Ripple Rejection vs Frequency

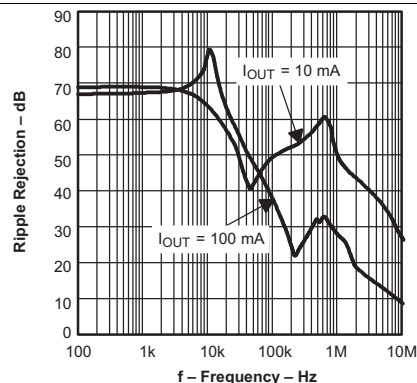
Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)



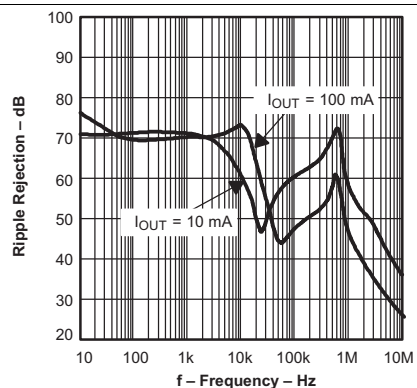
$V_{IN} = 2.8\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$

Figure 19. TPS79118 Ripple Rejection vs Frequency



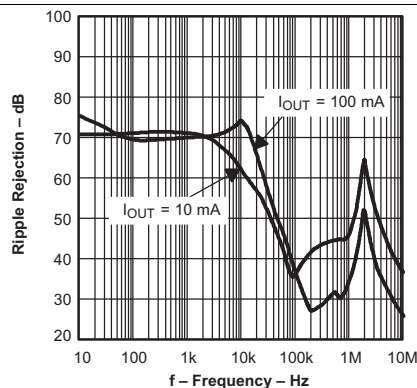
$V_{IN} = 2.8\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 20. TPS79118 Ripple Rejection vs Frequency



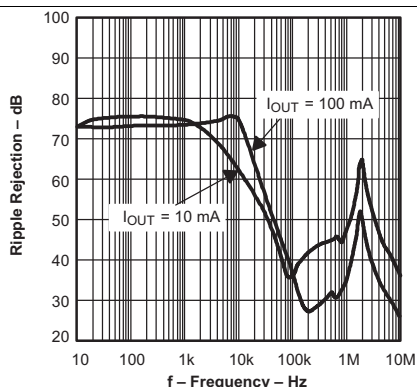
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$

Figure 21. TPS79133 Ripple Rejection vs Frequency



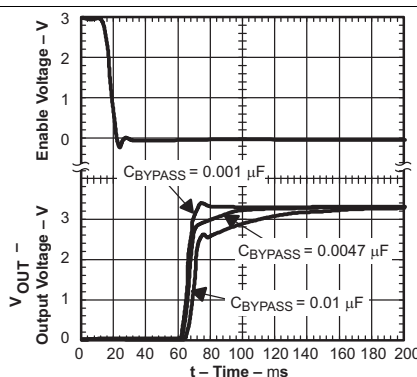
$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.01\text{ }\mu\text{F}$

Figure 22. TPS79133 Ripple Rejection vs Frequency



$V_{IN} = 4.3\text{ V}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $C_{BYPASS} = 0.1\text{ }\mu\text{F}$

Figure 23. TPS79133 Ripple Rejection vs Frequency



$V_{IN} = 4.3\text{ V}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 100\text{ mA}$, $C_{OUT} = 1\text{ }\mu\text{F}$, $T_J = 25^\circ\text{C}$

Figure 24. TPS79133 Output Voltage, Enable Voltage vs Time (Start-Up)

Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

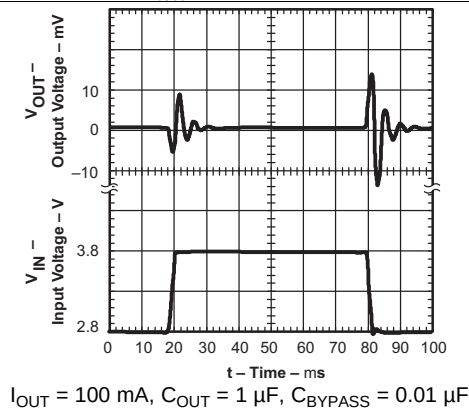


Figure 25. TPS79118 Line Transient Response

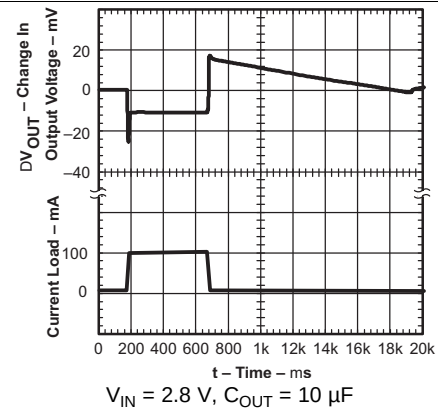


Figure 26. TPS79118 Load Transit Response

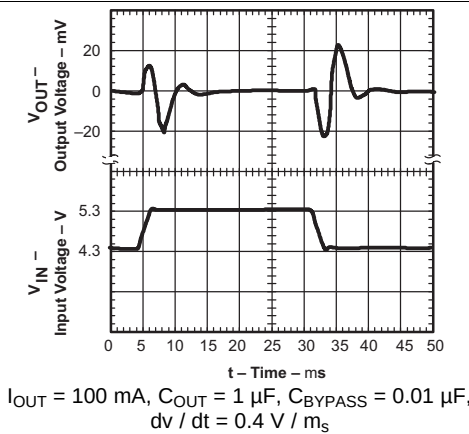


Figure 27. TPS79133 Line Transient Response

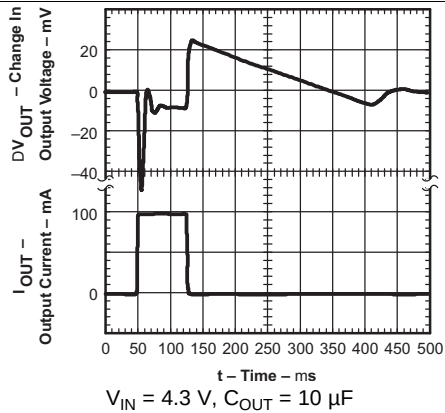


Figure 28. TPS79133 Load Transit Response

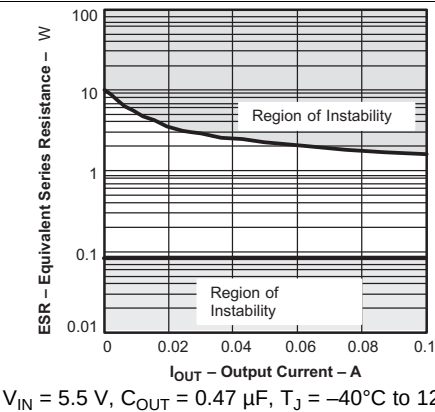


Figure 29. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

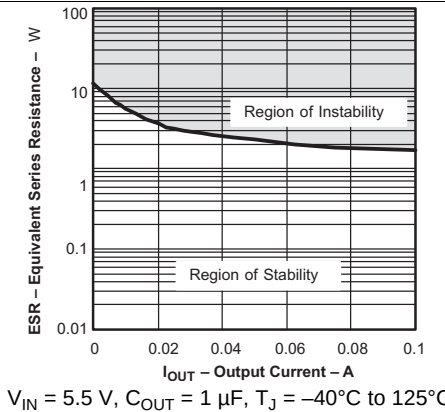


Figure 30. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $EN = 0\text{ V}$, $C_{OUT} = 10\text{ }\mu\text{F}$, and $C_{BYPASS} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted)

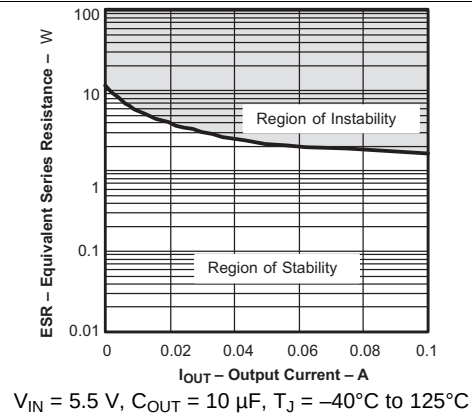


Figure 31. TPS79118 Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7.3 Feature Description

7.3.1 Power Dissipation and Junction Temperature

Specified regulator operation is confirmed at a junction temperature of 125°C; restrict the maximum junction temperature to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where

- T_{Jmax} is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the [Thermal Information](#) table)
- T_A is the ambient temperature

The regulator dissipation is calculated using:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

7.3.2 Programming the TPS79101 Adjustable Regulator

The output voltage of the TPS79101 adjustable regulator is programmed using an external resistor divider; see [Figure 32](#). The output voltage is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where

- $V_{REF} = 1.2246 \text{ V typ}$ (the internal reference voltage)

Select resistors R1 and R2 for approximately a 50-μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Avoid higher resistor values because leakage current into or out of FB across R1, R2 creates an offset voltage that artificially increases or decreases the feedback voltage and thus erroneously decreases or increases V_{OUT} . The recommended design procedure is to choose $R2 = 30.1 \text{ k}\Omega$ to set the divider current at 50 μA, $C1 = 15 \text{ pF}$ for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, a small compensation capacitor is suggested to be placed between OUT and FB. For voltages < 1.8 V, the value of this capacitor must be 100 pF. For voltages > 1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (5)$$

Feature Description (continued)

The table in Figure 34 shows the suggested value of this capacitor for several resistor ratios. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 2.2 μF instead of 1 μF .

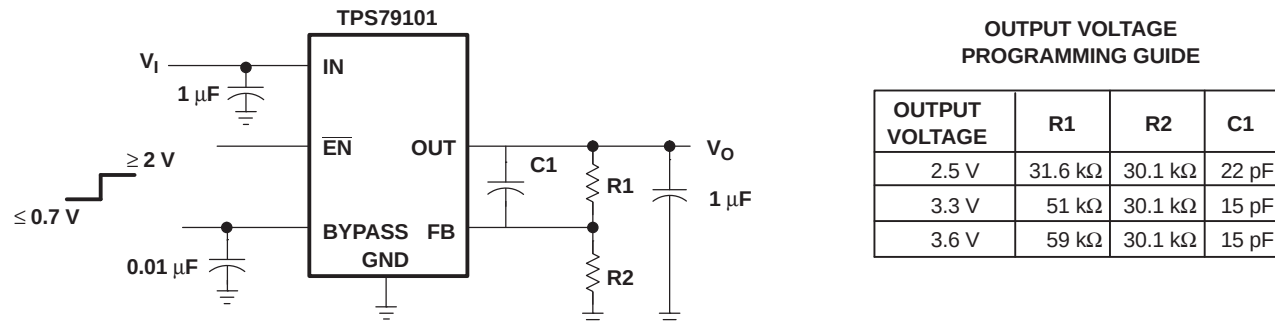


Figure 34. TPS79101 Adjustable LDO Regulator Programming

7.3.3 Regulator Protection

The TPS791 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting may be appropriate.

The TPS791 features internal current limiting and thermal protection. During normal operation, the TPS791 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Although current limiting is designed to prevent gross device failure, care must be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts the device down. When the device cools down to below approximately 140°C, regulator operation resumes.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as the $|V_{IN(min)}|$
- The input voltage magnitude is greater than the nominal output voltage magnitude added to the dropout voltage
- $|V_{EN}| < \text{low-level enable pin input voltage (0.7 V)}$
- The output current is less than the current limit
- The device junction temperature is less than the maximum specified junction temperature

7.4.2 Dropout Operation

If the input voltage magnitude is lower than the nominal output voltage magnitude plus the specified dropout voltage magnitude, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage magnitude is the same as the input voltage magnitude minus the dropout voltage magnitude. The transient performance of the device is significantly degraded because the pass device (such as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- $|V_{EN}| > \text{high-level enable pin input voltage (2 V)}$
- The device junction temperature is greater than the thermal shutdown temperature

[Table 1](#) shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$ V_{IN} > \{ V_{OUT(nom)} + V_{DO} , V_{IN(min)} \}$	$ V_{EN} < 0.7 \text{ V}$	$I_{OUT} < I_{CL}$	$T_J < 125^\circ\text{C}$
Dropout mode	$ V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO} $	$ V_{EN} < 0.7 \text{ V}$	—	$T_J < 125^\circ\text{C}$
Disabled mode (any true condition disables the device)	—	$ V_{EN} > 2 \text{ V}$	—	$T_J > 170^\circ\text{C}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS791 low-dropout (LDO) regulator is optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and an active-low, enable input to reduce supply currents to less than 1 μA when the regulator is turned off.

8.1.1 External Capacitor Requirements

A 0.1- μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS791, is required for stability and to improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

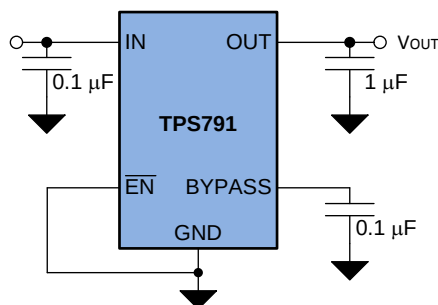
Like all low dropout regulators, the TPS791 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 μF . Any 1- μF or larger ceramic capacitor is suitable. The device is also stable with a 0.47- μF ceramic capacitor with at least 75 m Ω of ESR.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS791 has a BYPASS pin that is connected to the voltage reference through a 250-k Ω internal resistor. The 250-k Ω internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79118 exhibits approximately 15 μV_{RMS} of output voltage noise using a 0.1- μF ceramic bypass capacitor and a 1- μF ceramic output capacitor. The output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-k Ω resistor and external capacitor.

8.2 Typical Application

Figure 35 shows a typical application circuit.



Copyright © 2018, Texas Instruments Incorporated

Figure 35. Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

Table 2 shows the parameters used for this design example.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.3 V to 3.5 V (Lithium Ion battery)
Output voltage	3.3 V
DC output current	10 mA
Peak output current	100 mA
Maximum ambient temperature	60°C

8.2.2 Detailed Design Procedure

Select the desired output voltage option. An input capacitor of 0.1 μF is used because the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 1 mF is used in this design example. A smaller size output capacitor can be used up to a minimum of 1 μF to stabilize the internal control loop.

8.2.3 Application Curves

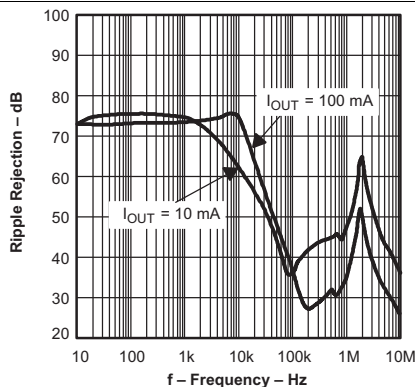


Figure 36. TPS79133 Ripple Rejection vs Frequency

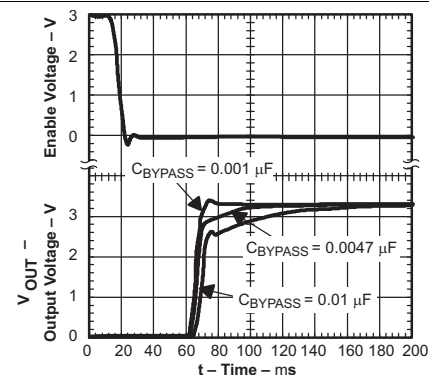


Figure 37. TPS79133 Output Voltage, Enable Voltage vs Time (Start-Up)

8.3 Do's and Don'ts

Do place at least one, low-ESR, 1- μF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low-ESR, 0.1- μF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the BYPASS pin.

Do not let the output voltage get more than 0.3 V above the input voltage.

9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1- μ F input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

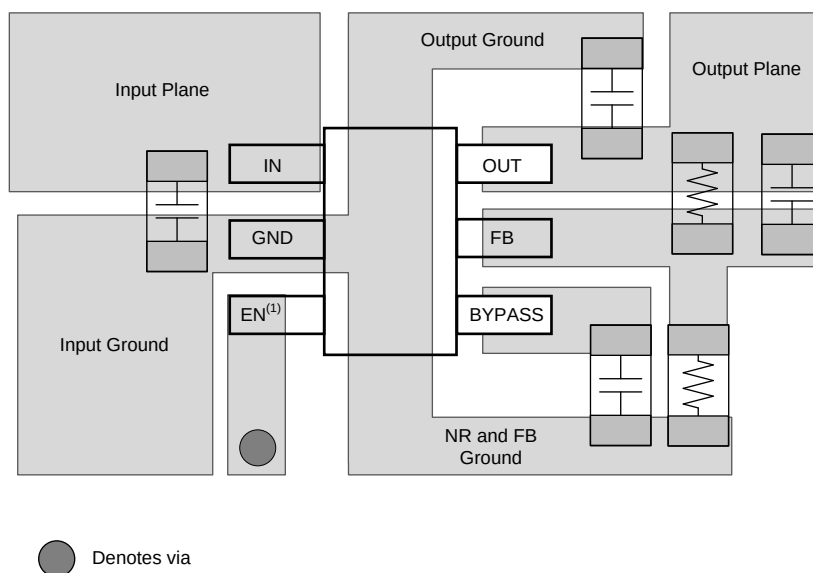
Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , C_{BYPASS} , and C_1) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits can impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements such as PSRR, output noise, and transient response, TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the ground pin of the device. In addition, connect the ground connection for the bypass capacitor directly to the ground pin of the device.

10.2 Layout Example



(1) The EN pin is active low.

Figure 38. Layout Example (6-Pin DBV Package)

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79101DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI	Samples
TPS79101DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI	Samples
TPS79101DBVT	LIFEBUY	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEUI	
TPS79118DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI	Samples
TPS79118DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI	
TPS79118DBVTG4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PERI	
TPS79133DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI	Samples
TPS79133DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI	Samples
TPS79133DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PESI	
TPS79147DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI	Samples
TPS79147DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI	
TPS79147DBVTG4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PETI	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS791 :

- Automotive : [TPS791-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

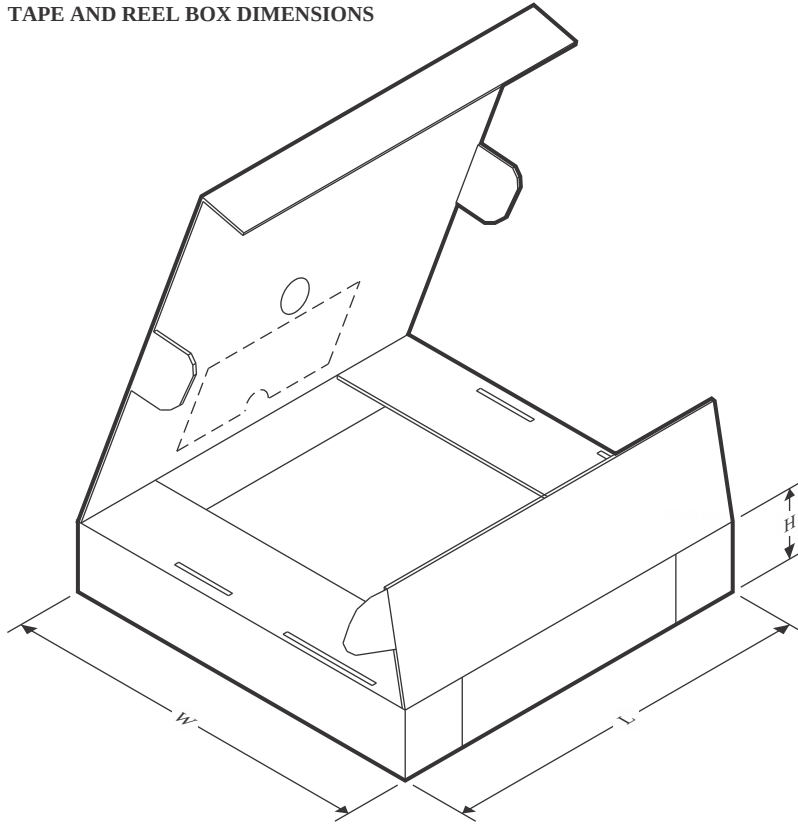
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79101DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79101DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79118DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79118DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79133DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79133DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79133DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS79147DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS79147DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79101DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS79101DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS79118DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79118DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS79133DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS79133DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79133DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS79147DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS79147DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

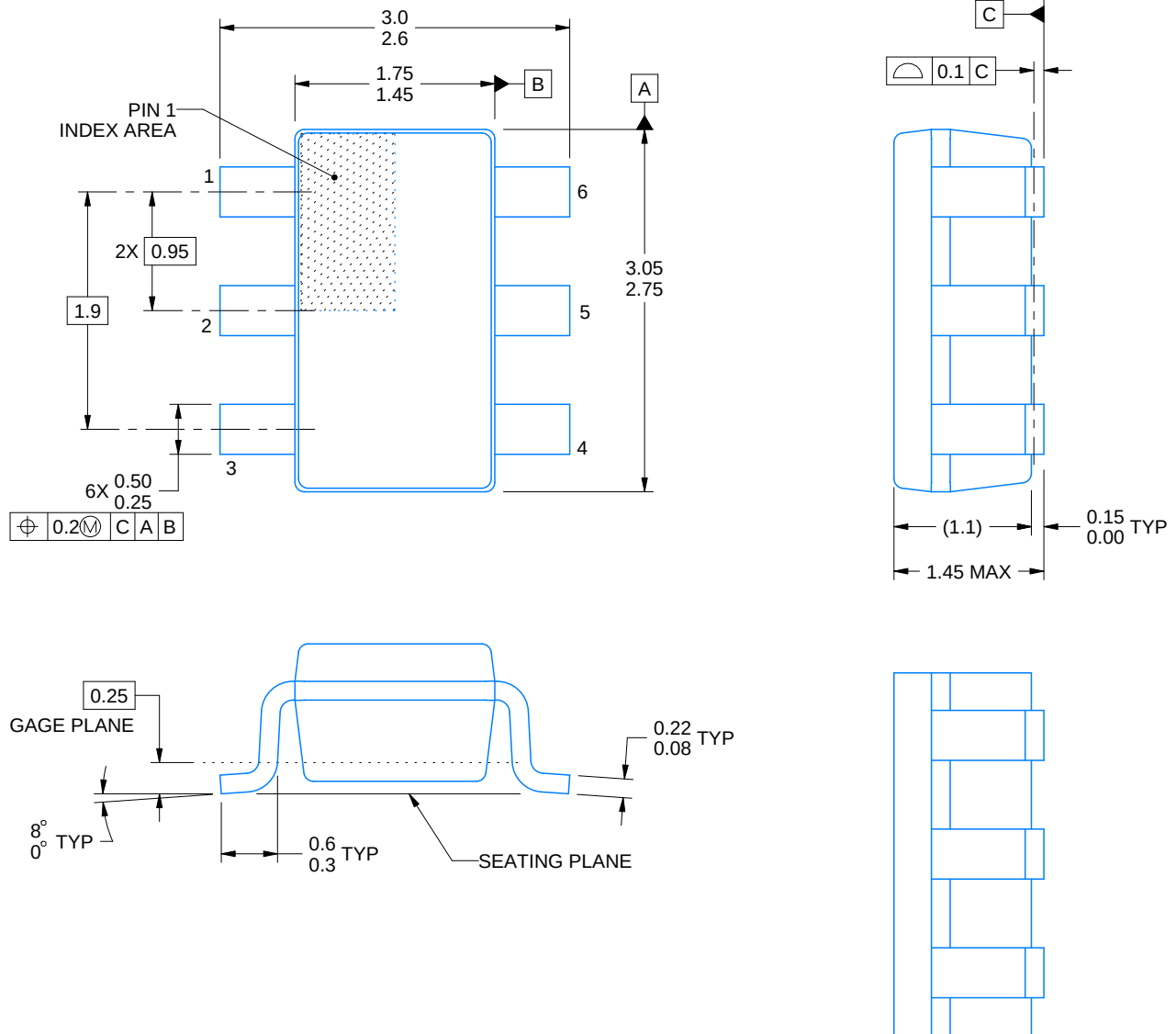
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/E 02/2024

NOTES:

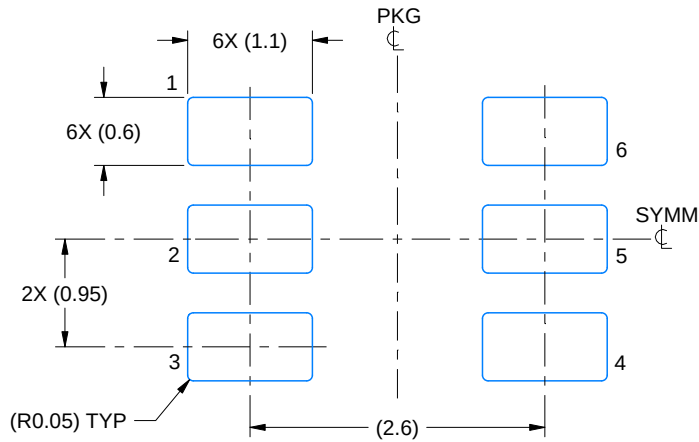
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

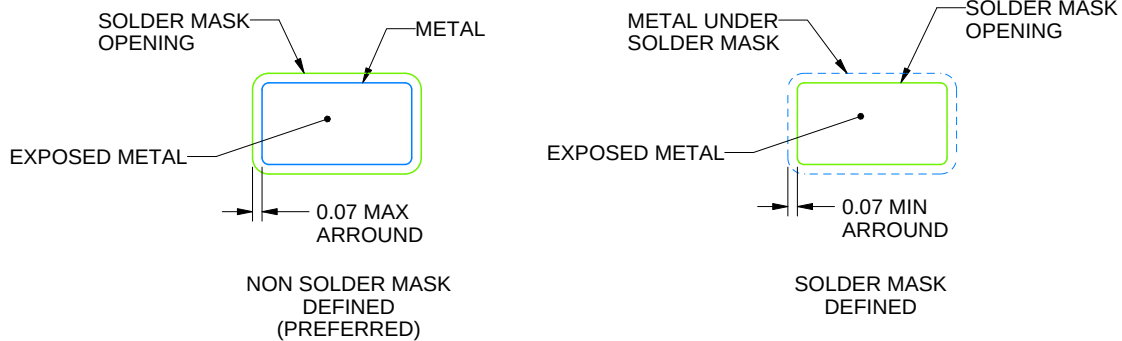
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

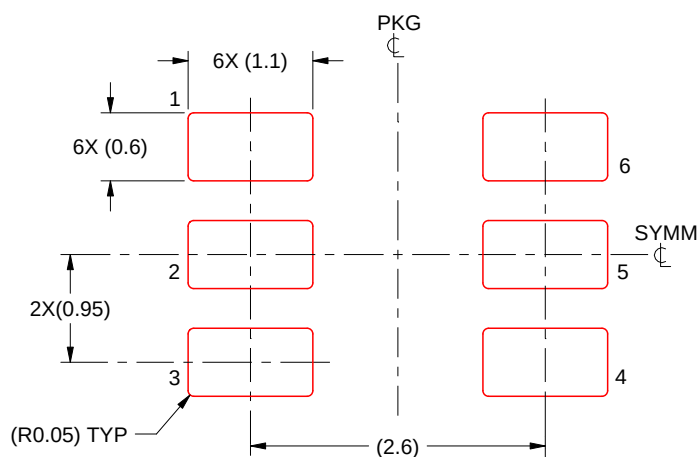
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

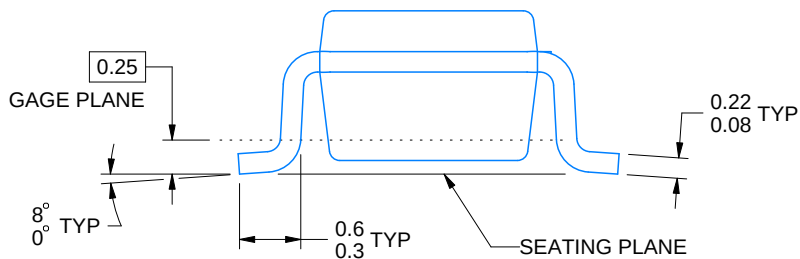
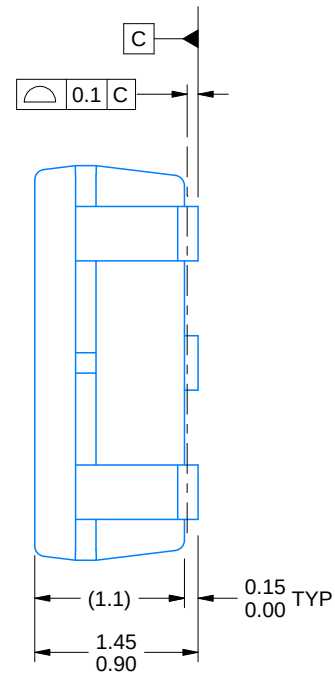
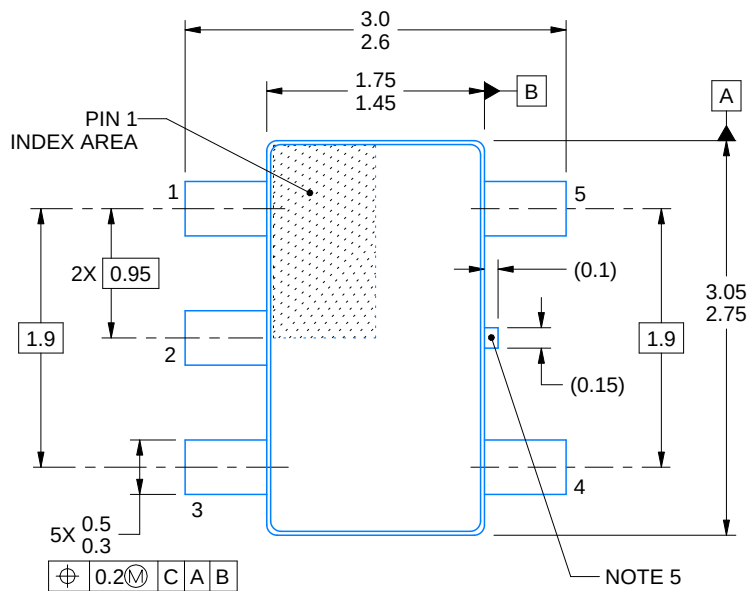
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

4214839/J 02/2024

NOTES:

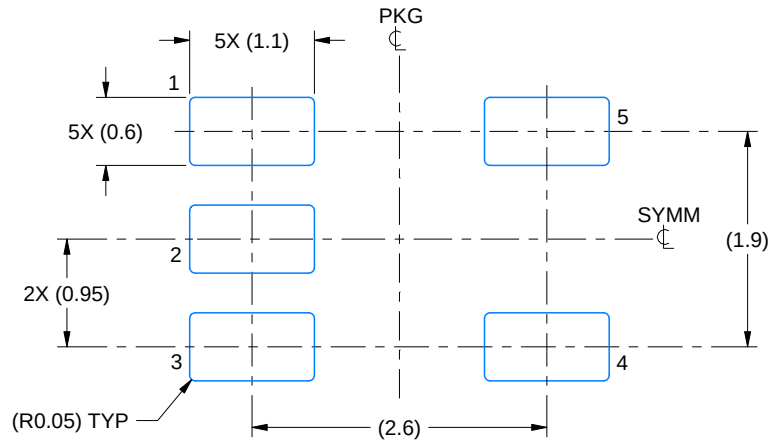
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

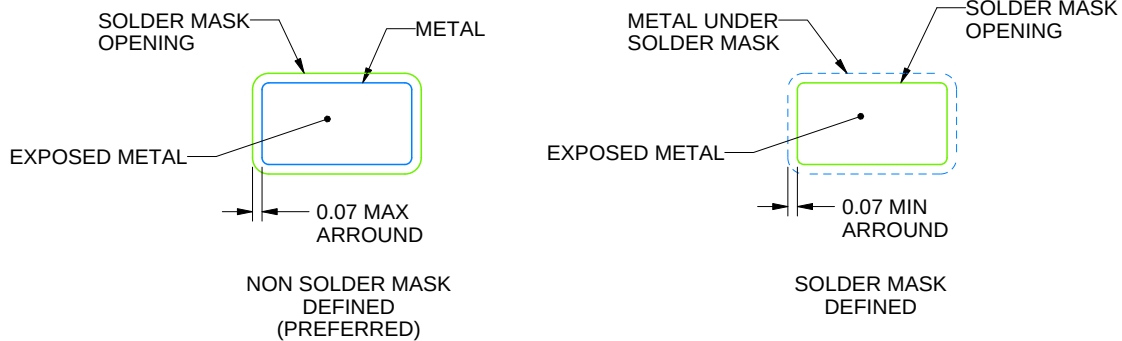
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

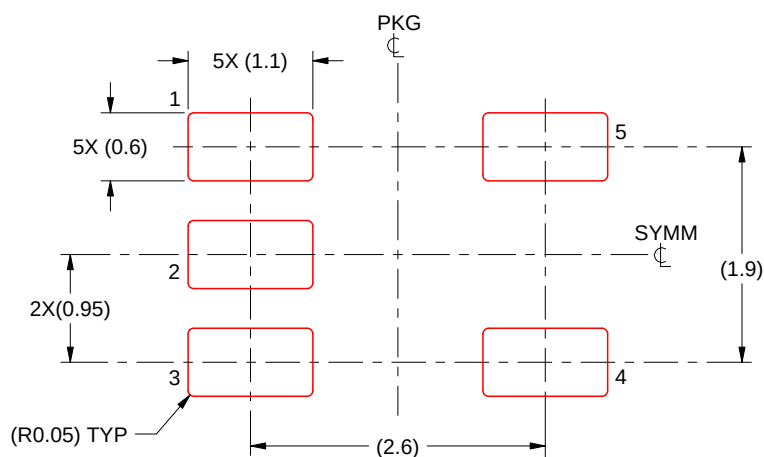
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated