TPS742
1.5A Ultra-LDO、ソフトスタートのプログラム可能

1 特長

- 入力電圧範囲: 0.8V～5.5V
- ソフトスタート(SS)ピンによりリニア・スタートアップを実現、ランプ時間は外部コンデンサにより設定
- ライン、負荷、温度の範囲にわたって1%の精度
- 外部バイアス電源により、最低0.8Vの入力電圧をサポート
- 可変出力(0.8V～3.6V)
- 非常に低いドロップアウト: 1.5Aにおいて55mV (標準値)
- 任意の出力コンデンサまたは出力コンデンサなしで安定
- 非常に優れた過渡応答
- オープン・ドレインのパワー・グッド(VQFN)
- アクティブHIGHイネーブル

2 アプリケーション

- FPGAアプリケーション
- DSPコアおよびI/O電圧
- サーバー
- ポスト・レギュレーション・アプリケーション
- 特別なスタートアップ時間やシーケンシングが必要なアプリケーション

3 概要

TPS742シリーズの低ドロップアウト(LDO)リニア・レギュレータは、広範なアプリケーション向けの使いやすく堅牢な電力管理ソリューションです。ソフトスタートをユーザーがプログラム可能なため、スタートアップ時の容量性負荷電流を低減して、入力電源のストレスを最小限に抑えることができます。ソフトスタートは単調性で、多くの種類のプロセッサやASICへの電源供給に適しています。イネーブル入力とパワー・グッド出力により、外部レギュレータとの間でシーケンシングを簡単に実行できます。この優れた柔軟性により、FPGA、DSP、および特殊なスタートアップ要件を持つ他のアプリケーションのシーケンス要件を満たすソリューションを構成できます。

高精度の基準電圧およびエラー・アンプは、負荷、ライン、温度、プロセス範囲にわたって1%の精度を維持します。各LDOは低コストのセラミック出力コンデンサで安定し、ファミリは-40℃～125℃までが完全に定格内です。TPS742デバイスは小型の5mm×5mm VQFN (RGW)、および小形の3.5mm×3.5mm VQFN (RGR)パッケージで供給され、ソリューション全体のサイズを減らすため役立ちます。

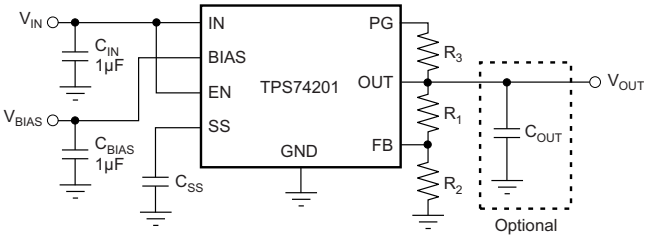
さらに大きい消費電力を必要とするアプリケーション向けに、DDPAK/TO-263 (KTW)パッケージも用意されています。

製品情報(1)

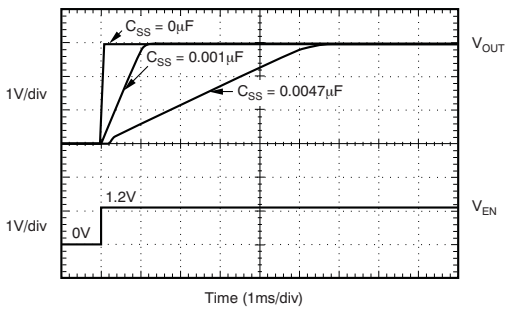
型番	パッケージ	本体サイズ(公称)
TPS74201	VQFN (20)、RGW	5.00mm×5.00mm
	VQFN (20)、RGR	3.50mm×3.50mm
	DDPAK/TO-263 (7)	8.89mm×10.10mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの可変出力バージョン



ターンオン応答



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision M (October 2015) から **Revision N** に変更 — **Page**

- ドキュメントにRGRパッケージを 追加 ... 1
- 「*特長*」のパッケージの箇条書き項目 削除 ... 1
- 「特長」のパワー・グッドの箇条書き項目 変更 ... 1
- 「*説明*」セクションの最後の段落にRGRパッケージを 追加 ... 1
- 「*製品情報*」表にRGRの行を 追加 ... 1
- Added RGR package to *Pin Configuration and Functions* section ... 4
- Changed pinout view of KTW package to *Top View* ... 4
- Added RGR package to *Thermal Information* table ... 6
- Changed Figure 32 title to reflect both VQFN packages instead of just one ... 21

Revision L (November 2010) から **Revision M** に変更 — **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Updated the value in Normal and Dropout modes under V_{BIAS} column ... 14

Revision K (August, 2010) から **Revision L** に変更 — **Page**

- Replaced the *Dissipation Ratings* table with the *Thermal Information* table ... 6
- Corrected equation for Table 2 ... 17
- Revised *Layout Recommendations and Power Dissipation* section ... 21

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Revision J (December, 2009) から Revision K に変更 **Page**

- Revised *Layout Guidelines* section 21
- Changed final paragraph of *Layout Guidelines* section..... 21
- Revised *Estimating Junction Temperature* section 22

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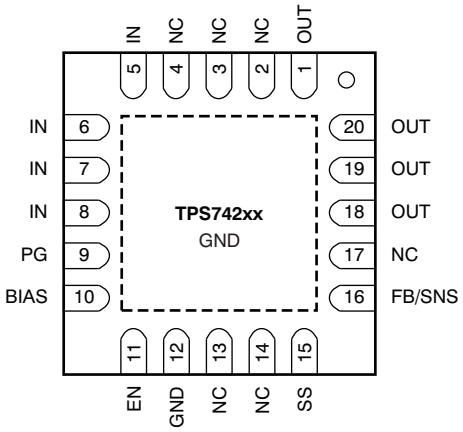
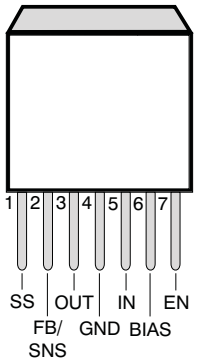
5 Pin Configuration and Functions

RGW, RGR Packages
20-Pin VQFN with Exposed Thermal Pad
Top View



KTW Package
7-Pin DDPAK/TO-263
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	KTW (DDPAK/ TO-263)	RGW, RGR (VQFN)		
BIAS	6	10	I	Bias input voltage for error amplifier, reference, and internal control circuits.
EN	7	11	I	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
FB	2	16	I	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating. (Adjustable version only.)
GND	4	12	—	Ground
IN	5	5,6,7,8	I	Unregulated input to the device.
NC	—	2, 3,4, 13,14,17	O	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
OUT	3	1, 18, 19, 20	O	Regulated output voltage. No capacitor is required on this pin for stability.
PAD/TAB	—	—	—	Solder to the ground plane for increased thermal performance.
PG	—	9	O	Power-Good (PG) is an open-drain, active-high output that indicates the status of V_{OUT}. When V_{OUT} exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When V_{OUT} is below this threshold the pin is driven to a low-impedance state. Connect a pullup resistor from 10 kΩ to 1 MΩ from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
SNS	2	16	I	This pin is the sense connection to the load device. This pin must be connected to V_{OUT} and must not be left floating. (Fixed versions only.)
SS	1	15	—	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left floating, the regulator output soft-start ramp time is typically 100 μs.

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6 Specifications

6.1 Absolute Maximum Ratings

at T_J = –40°C to 125°C (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
V_{IN}, V_{BIAS}	Input voltage	–0.3	6	V
V_{EN}	Enable voltage	–0.3	6	V
V_{PG}	Power-good voltage	–0.3	6	V
I_{PG}	PG sink current	0	1.5	mA
V_{SS}	SS pin voltage	–0.3	6	V
V_{FB}	Feedback pin voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum output current	Internally limited		
	Output short circuit duration	Indefinite		
P_{DISS}	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage junction temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	V_{OUT} + V_{DO}		5.5	V
V_{EN}	Enable supply voltage	0		5.5	V
V_{BIAS}(1)	BIAS supply voltage	V_{OUT} + V_{DO} (V_{BIAS})		5.5	V
I_{OUT}	Output current	0		1.5	A
C_{OUT}	Output capacitor	0			µF
C_{IN}(2)	Input capacitor	1			µF
C_{BIAS}	Bias capacitor	1			µF
T_J	Operating junction temperature	–40		125	°C

(1) BIAS supply is required when V_{IN} is below V_{OUT} + V_{DO} (V_{BIAS}).
(2) If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for the supply is 4.7 µF.

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6.4 Thermal Information

THERMAL METRIC[1][2][3]		TPS742			UNIT
		RGW (VQFN)	RGR (VQFN)	KTW (DDPAK/TO-263)	
		20 PINS	20 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	39.1	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	29.3	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.7	10.2	12.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.8	10.1	7.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	2.0	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the RGW, RGR, and KTW packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. RGW and RGR: The exposed pad is connected to the PCB ground layer through a 4 × 4 thermal via array.
ii. KTW: The exposed pad is connected to the PCB ground layer through a 6 × 6 thermal via array.
(b) Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, refer to the *Thermal Considerations* section.

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6.5 Electrical Characteristics

at V_{EN} = 1.1 V, V_{IN} = V_{OUT} + 0.3 V, C_{IN} = C_{BIAS} = 0.1 µF, C_{OUT} = 10 µF, I_{OUT} = 50 mA, V_{BIAS} = 5 V, and T_J = –40°C to 125°C (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage		2.375		5.25	V
V_{REF}	Internal reference (adjustable)	T_J = 25°C	0.796	0.8	0.804	V
V_{OUT}	Output voltage	V_{IN} = 5 V, I_{OUT} = 1.5 A, V_{BIAS} = 5 V	V_{REF}		3.6	V
	Accuracy(1)	2.375 V ≤ V_{BIAS} ≤ 5.25 V, V_{OUT} + 1.62 V ≤ V_{BIAS} 50 mA ≤ I_{OUT} ≤ 1.5 A	–1%	±0.2%	1%	
V_{OUT}/V_{IN}	Line regulation	$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V, VQFN		0.0005	0.05	%/V
		$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5 V, DDPAK/TO-263		0.0005	0.06	
V_{OUT}/I_{OUT}	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA		0.013		%/mA
		50 mA ≤ I_{OUT} ≤ 1.5 A		0.04		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62 V, VQFN		55	100	mV
		I_{OUT} = 1.5 A, V_{BIAS} – $V_{OUT\ (NOM)}$ ≥ 1.62 V, DDPAK/TO-263		60	120	
	V_{BIAS} dropout voltage(2)	I_{OUT} = 1.5 A, V_{IN} = V_{BIAS}			1.4	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT\ (NOM)}$	1.8		4	A
I_{BIAS}	Bias pin current	I_{OUT} = 0 mA to 1.5 A		2	4	mA
I_{SHDN}	Shutdown supply current (V_{IN})	V_{EN} ≤ 0.4 V		1	100	µA
I_{FB}, I_{SNS}	Feedback, Sense pin current(3)	I_{OUT} = 50 mA to 1.5 A	–250	68	250	nA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		73		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		42		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		62		dB
		300 kHz, I_{OUT} = 1.5 A, V_{IN} = 1.8 V, V_{OUT} = 1.5 V		50		
Noise	Output noise voltage	100 Hz to 100 kHz, I_{OUT} = 1.5 A, C_{SS} = 0.001 µF		16 × V_{OUT}		μV_{RMS}
V_{TRAN}	%V_{OUT} droop during load transient	I_{OUT} = 50 mA to 1.5 A at 1 A/µs, C_{OUT} = none		3.5		%V_{OUT}
t_{STR}	Minimum start-up time	I_{OUT} = 1.5 A, C_{SS} = open		100		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4 V	0.5	0.73	1	µA
$V_{EN,\ HI}$	Enable input high level		1.1		5.5	V
$V_{EN,\ LO}$	Enable input low level		0		0.4	V
$V_{EN,\ HYS}$	Enable pin hysteresis			50		mV
$V_{EN,\ DG}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5 V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	86.5	90	93.5	%V_{OUT}
V_{HYS}	PG trip hysteresis			3		%V_{OUT}
$V_{PG,\ LO}$	PG output low voltage	I_{PG} = 1 mA (sinking), V_{OUT} < V_{IT}			0.3	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG} = 5.25 V, V_{OUT} > V_{IT}		0.03	1	µA
T_J	Operating junction temperature		–40		125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		155		°C
		Reset, temperature decreasing		140		

(1) Adjustable devices tested at 0.8V; resistor tolerance is not taken into account.
(2) Dropout is defined as the voltage from the input to V_{OUT} when V_{OUT} is 2% below nominal.
(3) I_{FB}, I_{SNS} current flow is out of the device.

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6.6 Typical Characteristics

at T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, EN = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF (unless otherwise noted)

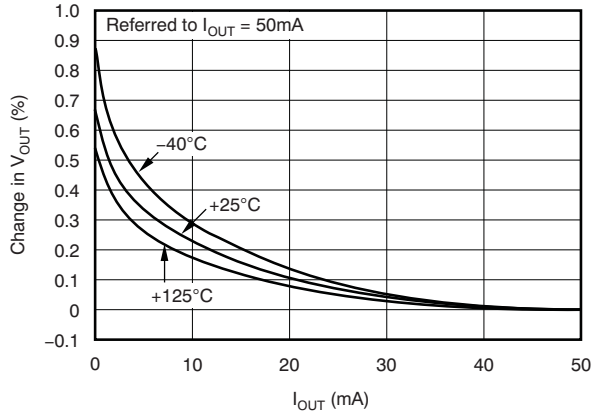

Figure 1. Load Regulation

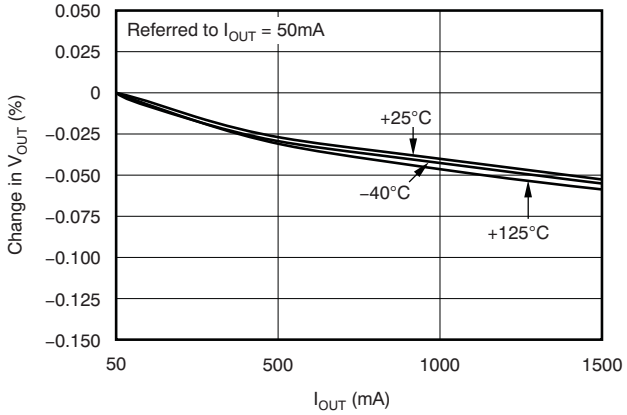

Figure 2. Load Regulation

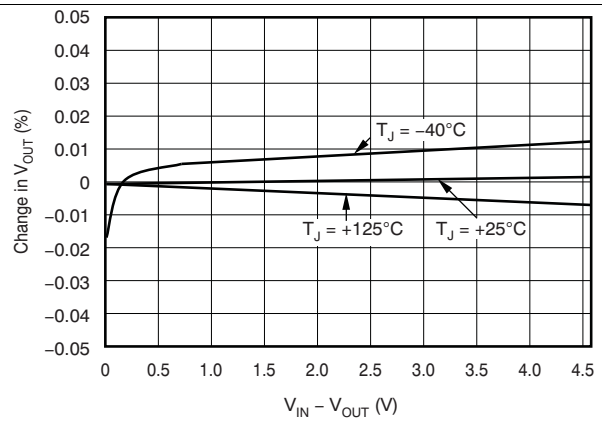

Figure 3. Line Regulation

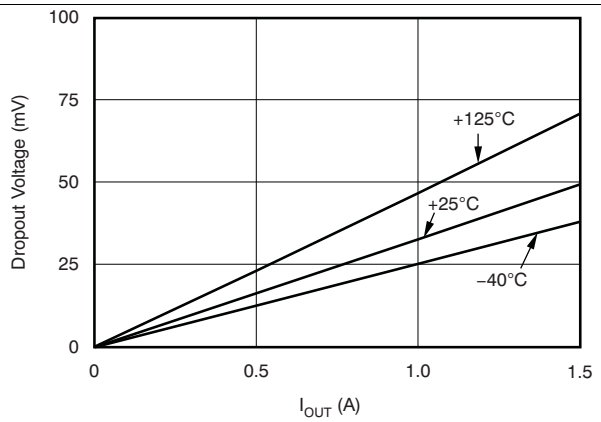

Figure 4. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

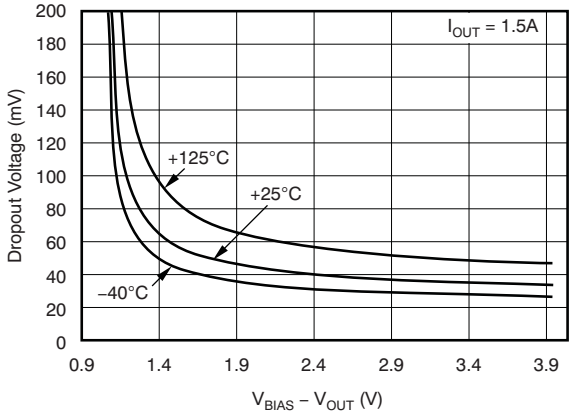

Figure 5. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)

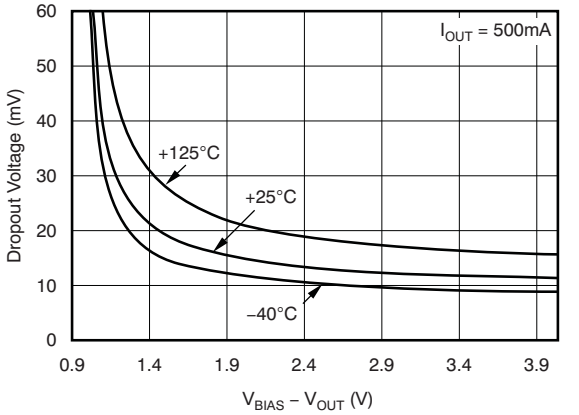

Figure 6. V_{IN} Dropout Voltage vs V_{BIAS} – V_{OUT} and Temperature (T_J)

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Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, EN = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF (unless otherwise noted)

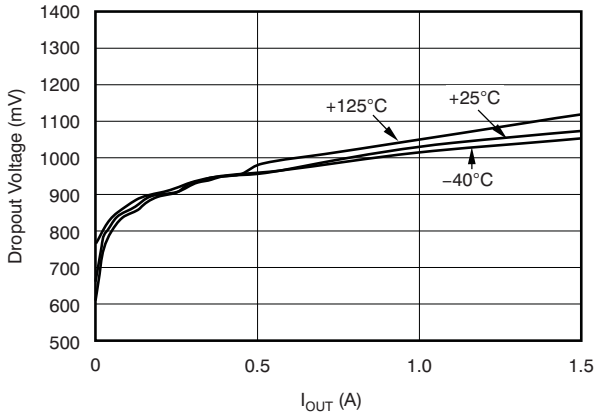

Figure 7. V_{BIAS} Dropout Voltage vs I_{OUT} and Temperature

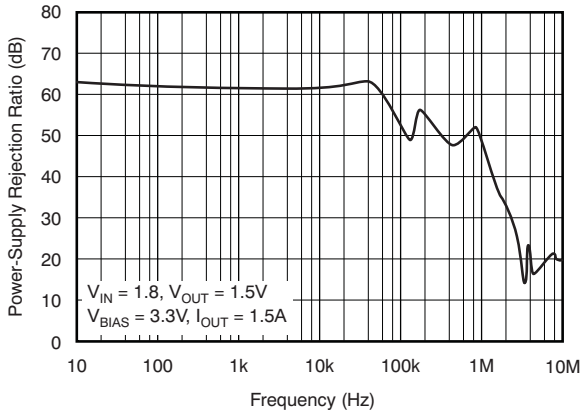

Figure 8. V_{BIAS} PSRR vs Frequency

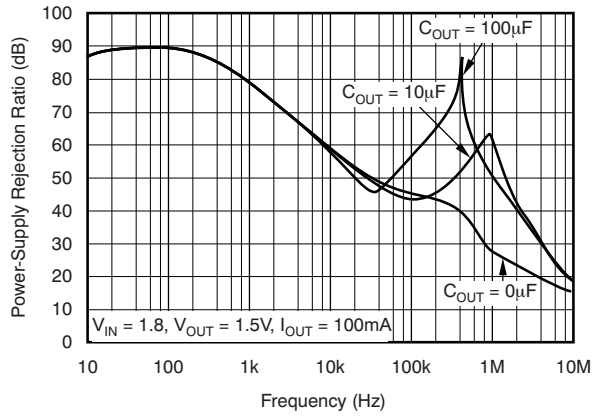

Figure 9. V_{IN} PSRR vs Frequency

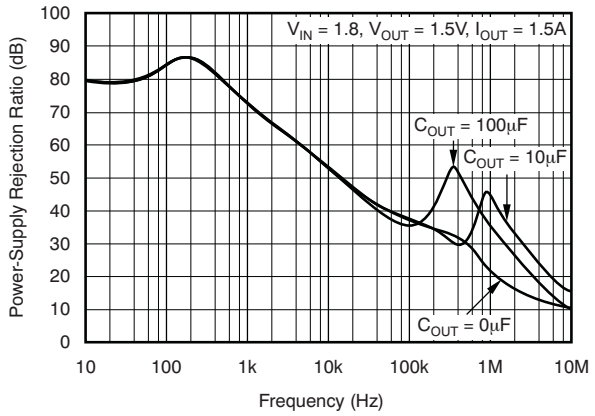

Figure 10. V_{IN} PSRR vs Frequency

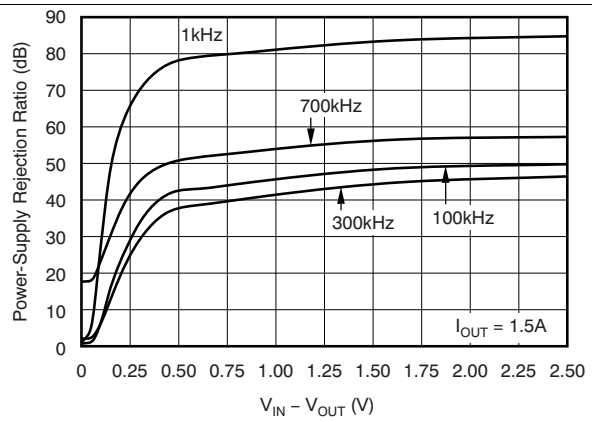

Figure 11. V_{IN} PSRR vs V_{IN} – V_{OUT}

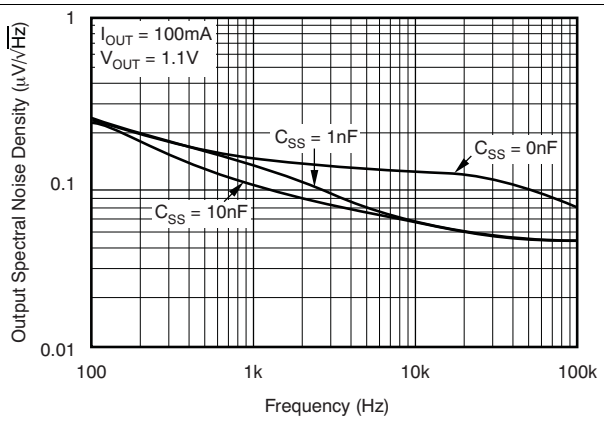

Figure 12. Noise Spectral Density

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Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, EN = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF (unless otherwise noted)

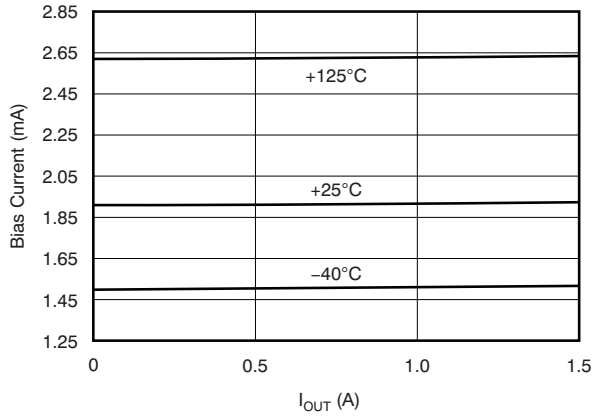

Figure 13. I_{BIAS} vs I_{OUT} and Temperature

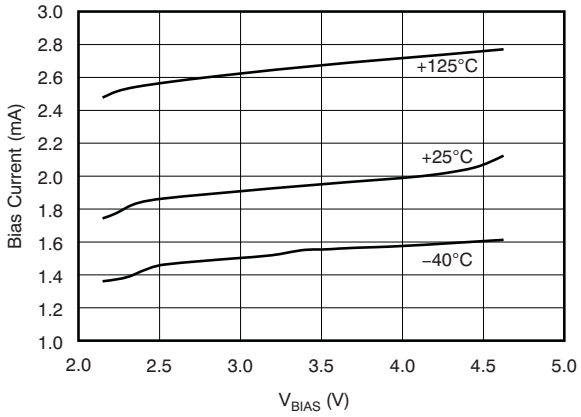

Figure 14. I_{BIAS} vs V_{BIAS} and V_{OUT}

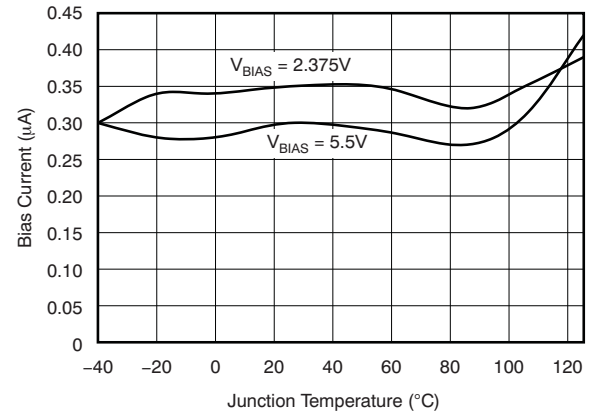

Figure 15. I_{BIAS} Shutdown vs Temperature

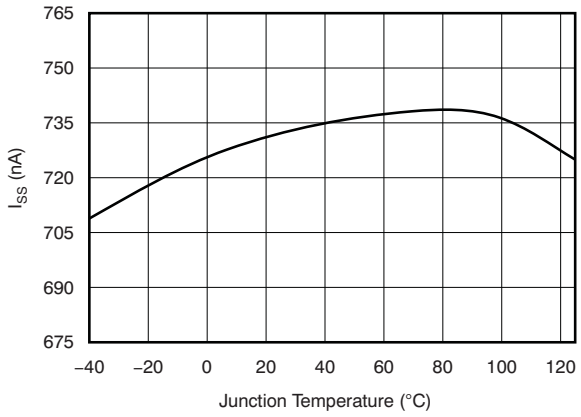

Figure 16. Soft-Start Charging Current (I_{SS}) vs Temperature

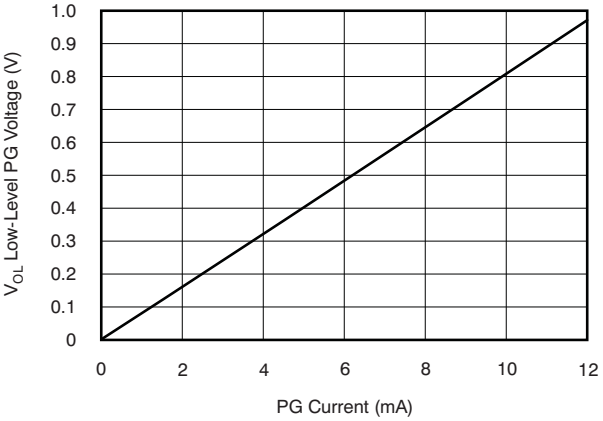

Figure 17. Low-Level PG Voltage vs PG Current

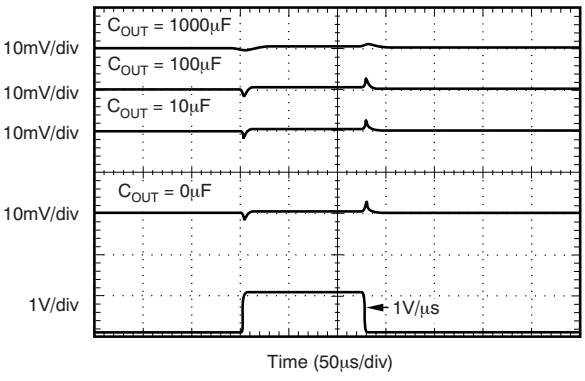

Figure 18. V_{BIAS} Line Transient (1.5 A)

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Typical Characteristics (continued)

at T_J = 25°C, V_{OUT} = 1.5 V, V_{IN} = $V_{OUT(TYP)}$ + 0.3 V, V_{BIAS} = 3.3 V, I_{OUT} = 50 mA, EN = V_{IN}, C_{IN} = 1 µF, C_{BIAS} = 4.7 µF, C_{SS} = 0.01 µF, and C_{OUT} = 10 µF (unless otherwise noted)

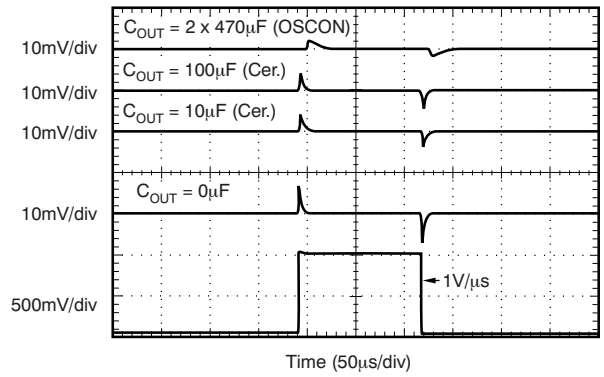


Figure 19. V_{IN} Line Transient

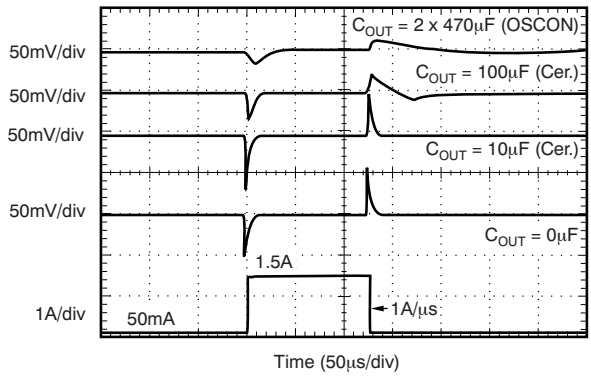


Figure 20. Output Load Transient Response

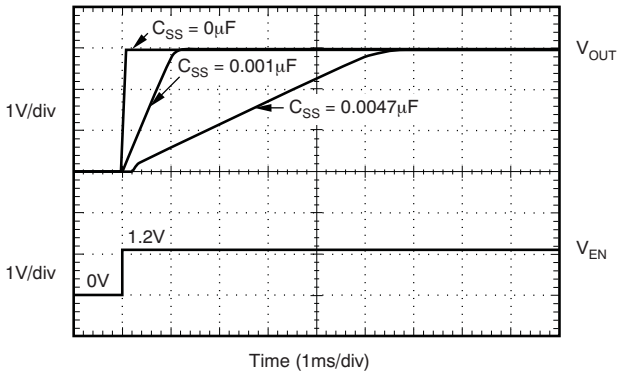


Figure 21. Turnon Response

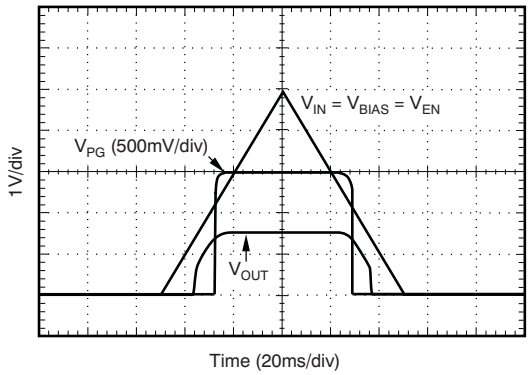


Figure 22. Power Up and Power Down

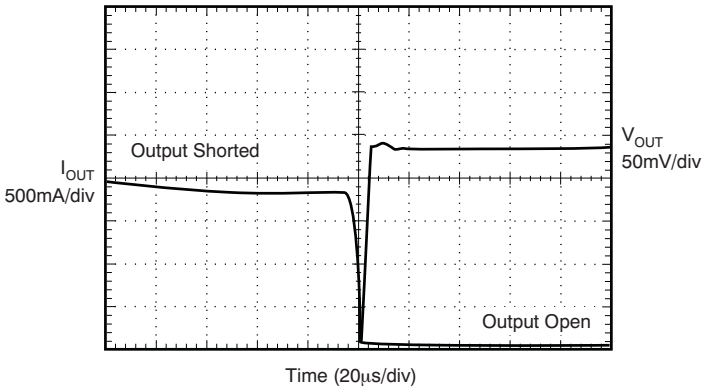


Figure 23. Output Short Circuit Recovery

7 Detailed Description

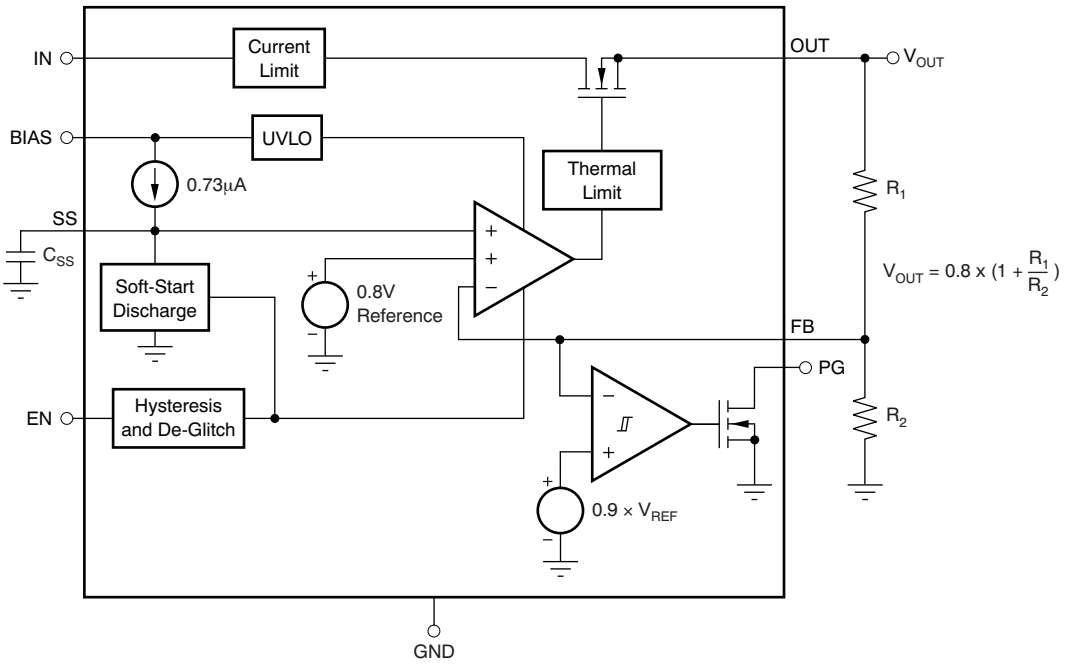
7.1 Overview

The TPS742 belongs to a family of generation ultra-low dropout regulators that feature soft-start and tracking capabilities. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS742 devices to be stable with any or even no output capacitor. Transient response is also superior to PMOS topologies, particularly for low V_{IN} applications.

The TPS742 devices feature a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits start-up inrush currents that may be caused by large capacitive loads. A power-good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low V_{IN} and V_{OUT} capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor intensive systems.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Enable and Shutdown

The enable (EN) pin is active high and is compatible with standard digital signaling levels. V_{EN} less than 0.4 V turns the regulator off and V_{EN} greater than 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slow-ramping analog signals. This configuration allows the TPS742 devices to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid ON and OFF cycling because of small glitches in the V_{EN} signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately –1 mV/°C; therefore, process variation accounts for most of the variation in the enable threshold. If precise turnon timing is required, then use a fast rise-time signal to enable the TPS742 devices.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, then connect EN as closely as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

7.3.2 Power-Good (VQFN Packages Only)

The power-good (PG) pin is an open-drain output and can be connected to any 5.5 V or lower rail through an external pullup resistor. This pin requires at least 1.1 V on V_{BIAS} to have a valid output. The PG output is high-impedance when V_{OUT} is greater than $V_{IT} + V_{HYS}$. If V_{OUT} drops below V_{IT} or if V_{BIAS} drops less than 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pullup resistor for PG must be in the range of 10 kΩ to 1 MΩ. PG is only provided on the VQFN packages. If output voltage monitoring is not needed, then the PG pin can be left floating.

7.3.3 Internal Current Limit

The TPS742 family features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 1.8 A and maintain regulation. The current limit responds in about 10 μs to reduce the current during a short circuit fault. Recovery from a short circuit condition is well-controlled and results in very little output overshoot when the load is removed. See Figure 23 in the *Typical Characteristics* section for a graph of I_{OUT} versus V_{OUT} performance.

The internal current limit protection circuitry of the TPS742 family of devices is designed to protect against overload conditions. The circuitry is not intended to allow operation above the rated current of the device. Continuously running the TPS742 devices above the rated current degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage and bias voltage are both at least at the respective minimum specifications.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.
- The device is not operating in dropout.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

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Device Functional Modes (continued)

7.4.3 Disabled

The device is disabled under the following conditions:

- The input or bias voltages are below the respective minimum specifications.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{EN}	V_{BIAS}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} \geq V_{OUT} + 1.4$ V	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$V_{IN} < V_{OUT(nom)} + V_{DO} (V_{IN})$	$V_{EN} > V_{EN(high)}$	$V_{BIAS} < V_{OUT} + 1.4$ V	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < V_{IN(min)}$	$V_{EN} < V_{EN(low)}$	$V_{BIAS} < V_{BIAS(min)}$	—	$T_J > 155°C$

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input, Output, and Bias Capacitor Requirements

The TPS742 family does not require any output capacitor for stability. If an output capacitor is needed, the device is designed to be stable for all available types and values of output capacitance. The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins is strongly dependent on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1μF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 μF. Use good quality, low ESR capacitors on the input; ceramic X5R and X7R capacitors are preferred. Place these capacitors as close to the pins as possible for optimum performance.

8.1.2 Transient Response

The TPS742 family of devices were designed to have transient response within 5% for most applications without any output capacitor. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient at the expense of a slightly longer V_{OUT} recovery time. See Figure 20 in the *Typical Characteristics* section. Because the TPS742 devices are stable without an output capacitor, many applications may allow for little or no capacitance at the LDO output. For these applications, local bypass capacitance for the device under power may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive high-value capacitors at the LDO output.

8.1.3 Dropout Voltage

The TPS742 family of devices offers industry-leading dropout performance, making this family well-suited for high-current low V_{IN}/low V_{OUT} applications. The extremely low dropout of the TPS742 allows the device to be used in place of a DC-DC converter and still achieve good efficiency. This efficiency allows the user to rethink the power architecture for their applications to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS742 devices. The first specification (illustrated in Figure 24) is referred to as *V_{IN} Dropout*, and is for users who wish to apply an external bias voltage to achieve low dropout. This specification assumes that V_{BIAS} is at least 1.62 V above V_{OUT}, which is the case for V_{BIAS} when powered by a 3.3-V rail with 5% tolerance and with V_{OUT} = 1.5 V. If V_{BIAS} is higher than 3.3 V × 0.95 or V_{OUT} is less than 1.5 V, V_{IN} dropout is less than specified.

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Application Information (continued)

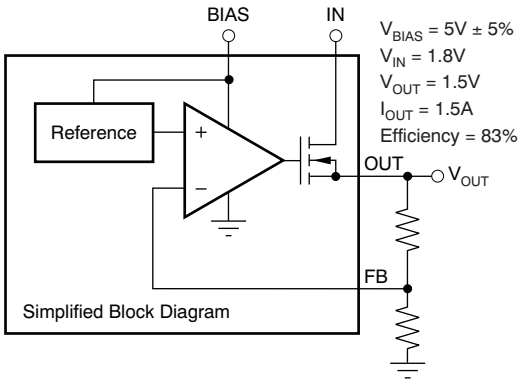

Figure 24. Typical Application of the TPS742 Using an Auxiliary Bias Rail

The second specification (shown in Figure 25) is referred to as *V_{BIAS} Dropout*, and is for users who wish to tie IN and BIAS together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because V_{BIAS} provides the gate drive to the pass FET and therefore must be 1.4 V above V_{OUT}. Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

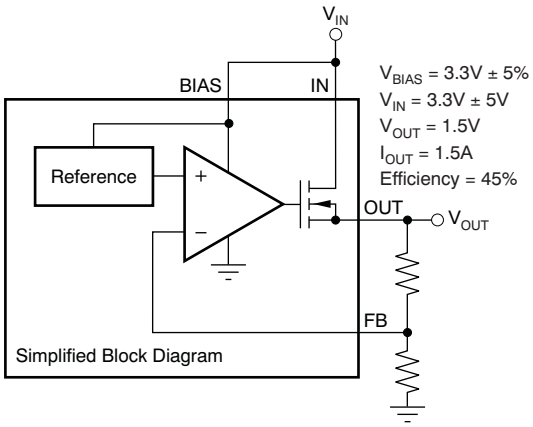

Figure 25. Typical Application of the TPS742 Without an Auxiliary Bias

8.1.4 Output Noise

The TPS742 devices provide low-output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001-µF soft-start capacitor, the output noise is reduced by half and is typically 30 μV_{RMS} for a 1.2-V output (10 Hz to 100 kHz). Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001-µF soft-start capacitor is given in Equation 1.

$$V_N\left(\mu V_{RMS}\right) = 25\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}\ (V) \tag{1}$$

The low-output noise of the TPS742 makes the device a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

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Application Information (continued)

8.1.5 Programmable Soft-Start

The TPS742 devices feature a programmable, monotonic, voltage-controlled soft start that is set with an external capacitor (C_{SS}). This feature is important for many applications, because power-up initialization problems are eliminated when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transients to the input power bus.

To achieve a linear and monotonic soft-start, the TPS742 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}), and can be calculated using Equation 2:

$$t_{SS} = \frac{(V_{REF} \times C_{SS})}{I_{SS}} \quad (2)$$

If large output capacitors are used, the device current limit (I_{CL}) and the output capacitor may set the start-up time. In this case, the start-up time is given by Equation 3:

$$t_{SSCL} = \frac{(V_{OUT(NOM)} \times C_{OUT})}{I_{CL(MIN)}} \quad (3)$$

$V_{OUT(NOM)}$ is the nominal set output voltage as set by the user, C_{OUT} is the output capacitance, and $I_{CL(MIN)}$ is the minimum current limit for the device. In applications where monotonic start-up is required, the soft-start time given by Equation 2 must be set to be greater than Equation 3.

The maximum recommended soft-start capacitor is 0.015 μF. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 0.015 μF could be a problem in applications where the user must rapidly pulse the enable pin and still requires the device to soft-start from ground. C_{SS} must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. See Table 2 for suggested soft-start capacitor values.

Table 2. Standard Capacitor Values for Programming the Soft-Start Time (See Equation 4)

C_{SS}	SOFT-START TIME
Open	0.1 ms
470 pF	0.5 ms
1000 pF	1 ms
4700 pF	5 ms
0.01 μF	10 ms
0.015 μF	16 ms

$$t_{SS}(s) = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8V \times C_{SS}(F)}{0.73\mu A} \quad (4)$$

where

- $t_{SS}(s)$ = soft-start time in seconds

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8.1.6 Sequencing Requirements

The device can have V_{IN}, V_{BIAS}, and V_{EN} sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Enabling the device after V_{IN} and V_{BIAS} are present is preferred, and can be accomplished using a digital output from a processor or supply supervisor. An analog signal from an external RC circuit, as shown in Figure 26, can also be used as long as the delay time is long enough for V_{IN} and V_{BIAS} to be present.

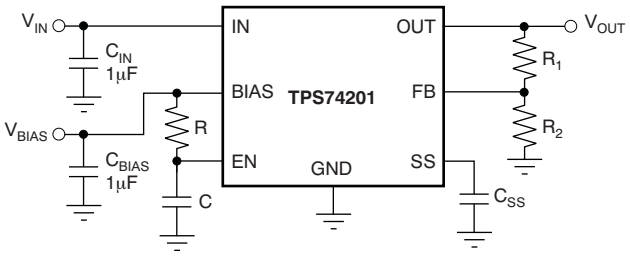

Figure 26. Soft-Start Delay Using an RC Circuit on Enable

If a signal is not available to enable the device after IN and BIAS, simply connecting EN to IN is acceptable for most applications as long as V_{IN} is greater than 1.1 V and the ramp rate of V_{IN} and V_{BIAS} is faster the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until the set output voltage is reached. If EN is connected to BIAS, the device does soft-start as programmed provided that V_{IN} is present before V_{BIAS}. If V_{BIAS} and V_{EN} are present before V_{IN} is applied and the set soft-start time has expired then V_{OUT} tracks V_{IN}.

NOTE

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition will not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ..

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8.2 Typical Applications

Figure 27 is a typical application circuit for the TPS742 adjustable output device.

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 27. See Table 3 for sample resistor values of common output voltages. To achieve the maximum accuracy specifications, R_2 must be ≤ 4.99 kΩ.

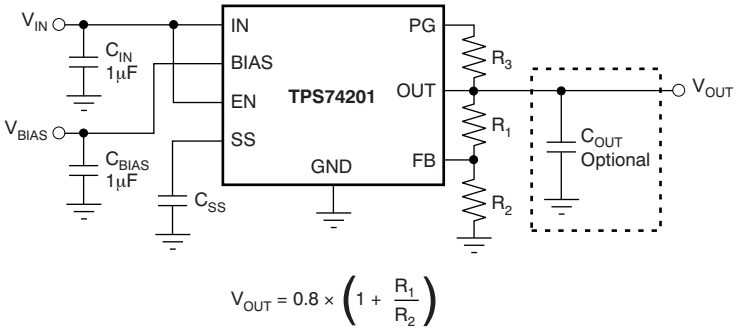

Figure 27. Typical Application Circuit for the TPS742

Table 3. Standard 1% Resistor Values for Programming the Output Voltage (See Equation 5)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

$$V_{OUT} = 0.8 \times (1 + R1/R2) \quad (5)$$

NOTE

When V_{BIAS} and V_{EN} are present and V_{IN} is not supplied, this device outputs approximately 50 µA of current from OUT. Although this condition does not cause any damage to the device, the output current can charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 kΩ.

8.2.1 Design Requirements

The design goals are V_{IN} = 1.8 V, V_{OUT} = 1.5 V, and I_{OUT} = 1 A (maximum). The design optimizes transient response and meets a 1-ms start-up time with a start-up dominated by the soft-start feature. The input supply comes from a supply on the same circuit board. The available system rails for V_{BIAS} are 2.7 V, 3.3 V, and 5 V.

The design space consists of C_{IN}, C_{OUT}, C_{BIAS}, C_{SS}, V_{BIAS}, R_1, R_2, and R_3, and the circuit is from Figure 27.

This example uses a V_{IN} of 1.8 V, with a V_{BIAS} of 2.5 V.

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8.2.2 Detailed Design Procedure

This is assuming the table for the standard capacitor values is put back in as Table 1.

Utilizing Table 3, we select R1 = 4.12 kΩ for V_{OUT} = 1.5 V. and R2 = 4.75 kΩ. Using Table 1, we select C_{SS} = 1000 pF for a 1-ms typical start-up time. For optimal performance, we use the 5-V rail for a Bias supply. An R3 of 100 kΩ is selected as the PG bus is used by other devices with additional 100-kΩ pullup resistors.

A C_{IN} of 10 µF is used for better transient performance on the input supply, a C_{BIAS} of 1 µF is used to ensure the Bias supply is solid, and a C_{OUT} of 1 µF is used to provide some local capacitance on the output.

8.2.3 Application Curves

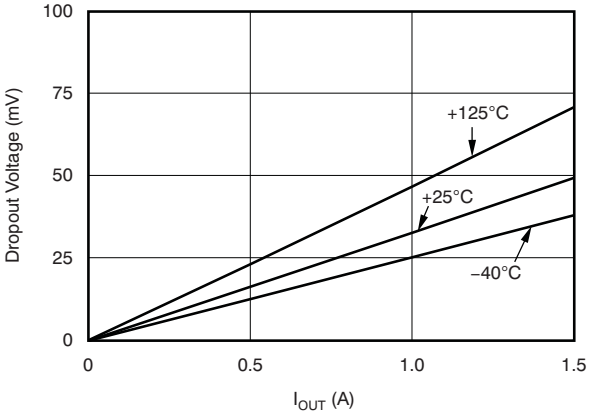

Figure 28. V_{IN} Dropout Voltage vs I_{OUT} and Temperature (T_J)

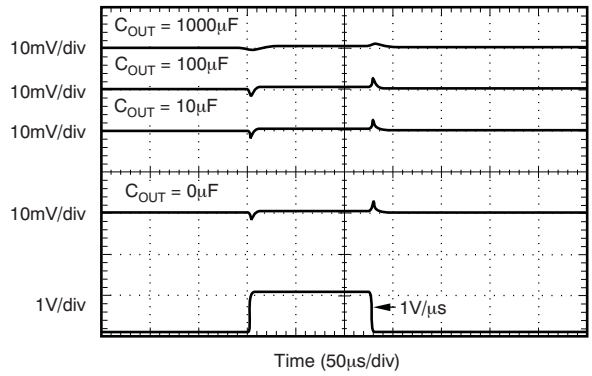

Figure 29. V_{BIAS} Line Transient (1.5 A)

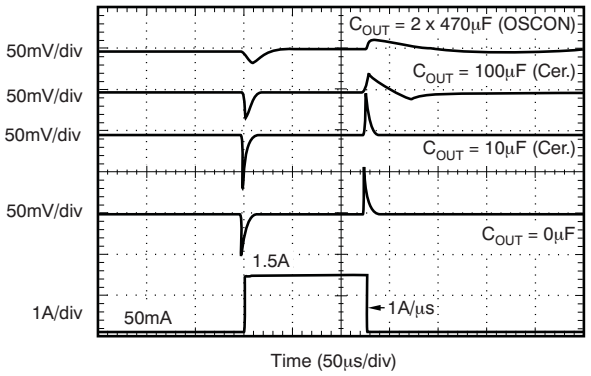

Figure 30. Output Load Transient Response

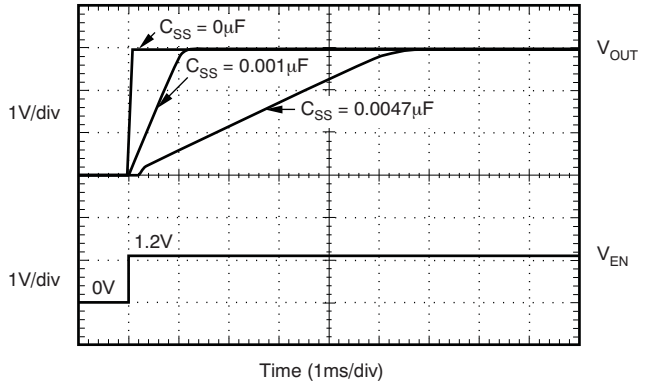

Figure 31. Turnon Response

9 Power Supply Recommendations

The TPS742 devices are designed to operate from an input voltage from 1.1 V to 5.5 V, provided the bias rail is at least 1.4-V higher than the input supply. The bias rail and the input supply must both provide adequate headroom and current for the device to operate normally.

Connect a low-output impedance power supply directly to the IN pin of the TPS742 devices. This supply must have at least 1 µF of capacitance near the IN pin for stability. A supply with similar requirements must also be connected directly to the bias rail with a separate 1 µF or larger capacitor.

If the IN pin is tied to the bias pin, a minimum 4.7 µF of capacitance is needed for stability.

To increase the overall PSRR of the solution at higher frequencies, use a pi-filter or ferrite bead before the input capacitor.

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10 Layout

10.1 Layout Guidelines

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage droop on the input of the device during load transients, connect the capacitance on IN and BIAS as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can therefore improve stability. To achieve optimal transient performance and accuracy, connect the top side of R_1 in Figure 27 as close as possible to the load. If BIAS is connected to IN, TI recommends connecting BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage droop on BIAS during transient conditions and can improve the turnon response.

10.2 Layout Example

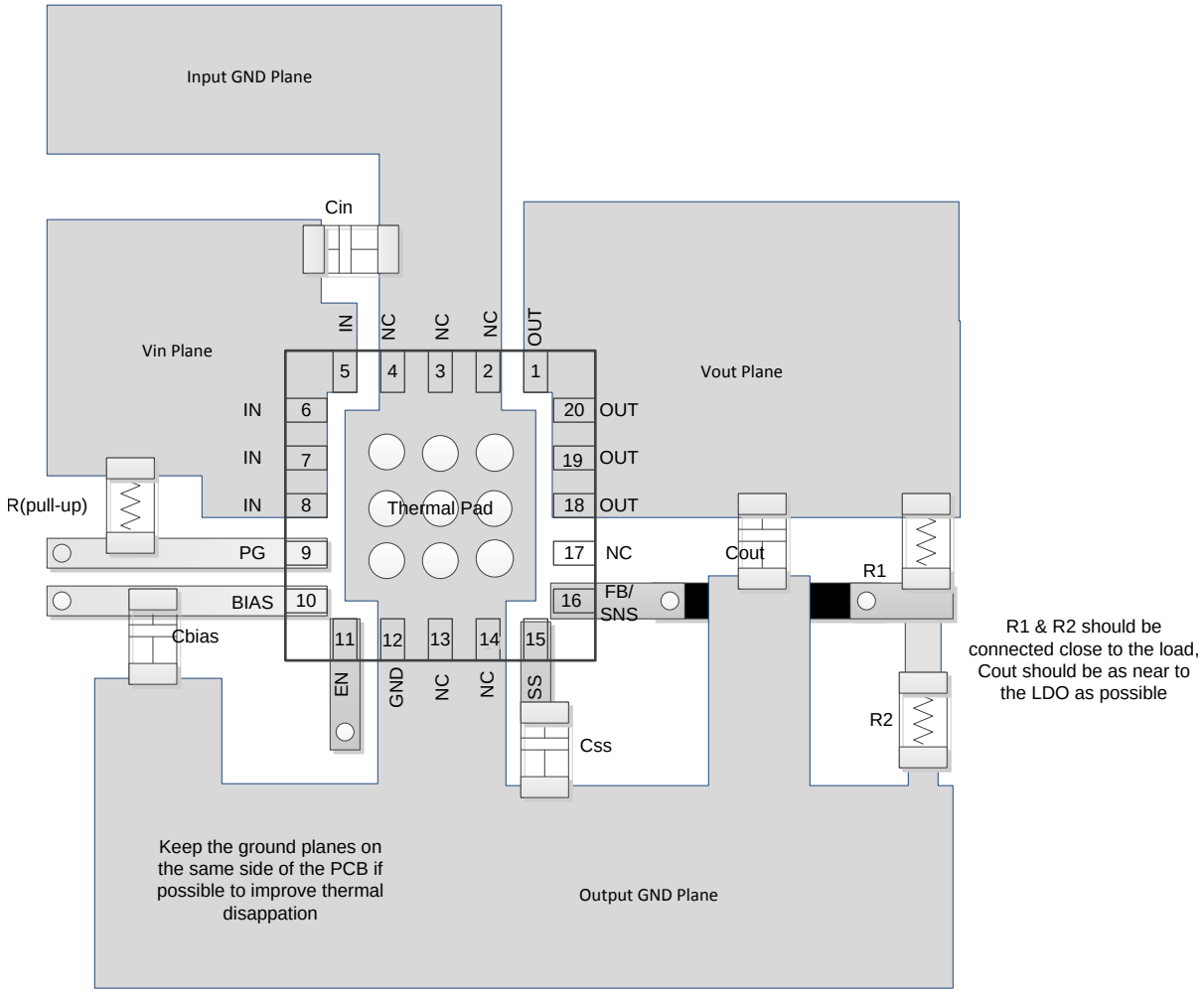

Figure 32. Layout Schematic (VQFN Packages)

10.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS742 devices is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS742 devices into thermal shutdown degrades device reliability.

10.4 Thermal Considerations

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in *Thermal Information*, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older θ_{JC},Top parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D \tag{6}$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D$$

where

- P_D is the power dissipation given by $P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$
- T_T is the temperature at the center-top of the IC package
- T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 33 shows).

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

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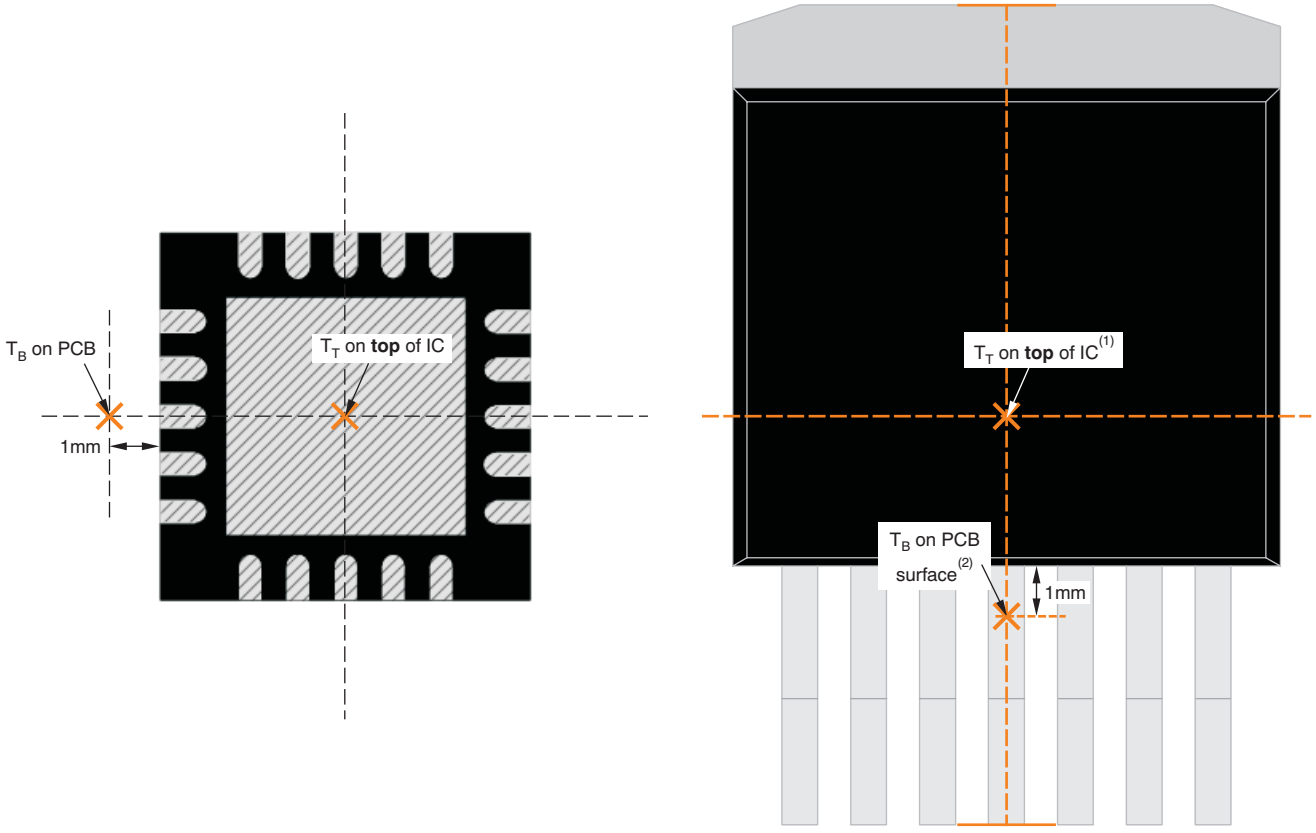
Thermal Considerations (continued)



(a) Example RGW (QFN) Package Measurement **(b) Example KTW (DDPAK) Package Measurement**

(1) T_T is measured at the center of both the X- and Y-dimensional axes.
(2) T_B is measured ***below*** the package lead **on the PCB surface**.

Figure 33. Measuring Points for T_T and T_B

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Thermal Considerations (continued)

Compared with θ_{JA}, the new thermal metrics Ψ_{JT} and Ψ_{JB} are less independent of board size, but they do have a small dependency. Figure 34 shows characteristic performance of Ψ_{JT} and Ψ_{JB} versus board size.

Looking at Figure 34, the RGW package thermal performance has negligible dependency on board size. The KTW package, however, does have a measurable dependency on board size. This dependency exists because the package shape is not point-symmetric to an IC center. In the KTW package, for example (see Figure 33), silicon is not beneath the measuring point of T_T, which is the center of the X and Y dimension, so that Ψ_{JT} has a dependency. Also, because of that non-point-symmetry, device heat distribution on the PCB is not point-symmetric, either, so that Ψ_{JB} has a dependency.

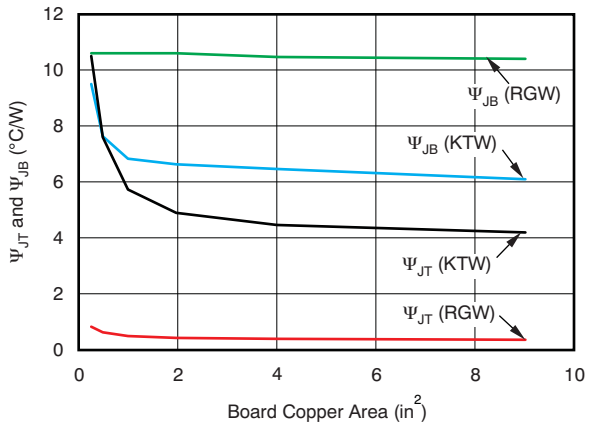

Figure 34. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using θ_{JC},Top to determine thermal characteristics, refer to the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com. Also, refer to the application note *IC Package Thermal Metrics* (SPRA953) (also available on the TI website) for further information.

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 開発サポート

11.1.1.1 評価モジュール

TPS744を使用する回路の性能の初期評価に役立てるため、評価モジュール(EVM)を利用可能です。TPS74201EVM-118評価モジュール(および関連するユーザー・ガイド)は、テキサス・インスツルメンツのWebサイトの製品フォルダから請求するか、TI eStoreから直接お求めになれます。

11.1.1.2 SPICEモデル

SPICEを使用した回路パフォーマンスのコンピュータによるシミュレーションは、アナログ回路やシステムのパフォーマンスを分析するため多くの場合に有用です。TPS744用のSPICEモデルは、製品フォルダの「ツールとソフトウェア」から入手できます。

11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『6A電流共有デュアルLDO』*
- *『新しい熱測定基準の使用』アプリケーション・レポート*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

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11.7 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

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12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74201KTWR	ACTIVE	DDPAK/ TO-263	KTW	7	500	RoHS & Green	Call TI | SN	Level-3-245C-168 HR	-40 to 125	TPS74201	Samples
TPS74201KTWRG3	ACTIVE	DDPAK/ TO-263	KTW	7	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	TPS74201	Samples
TPS74201RGRR	ACTIVE	VQFN	RGR	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12JA	Samples
TPS74201RGRT	LIFEBUY	VQFN	RGR	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12JA	
TPS74201RGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74201	Samples
TPS74201RGWRG4	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74201	Samples
TPS74201RGWT	ACTIVE	VQFN	RGW	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74201	Samples
TPS74201RGWTG4	ACTIVE	VQFN	RGW	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 74201	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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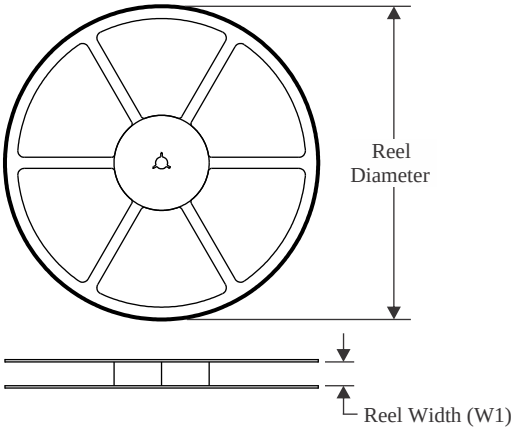
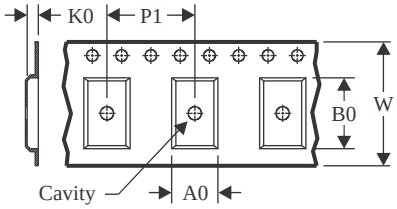
TAPE AND REEL INFORMATION

REEL DIMENSIONS

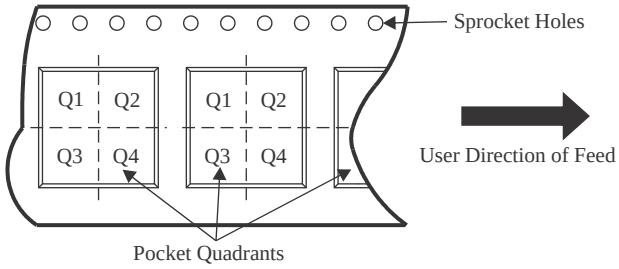


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

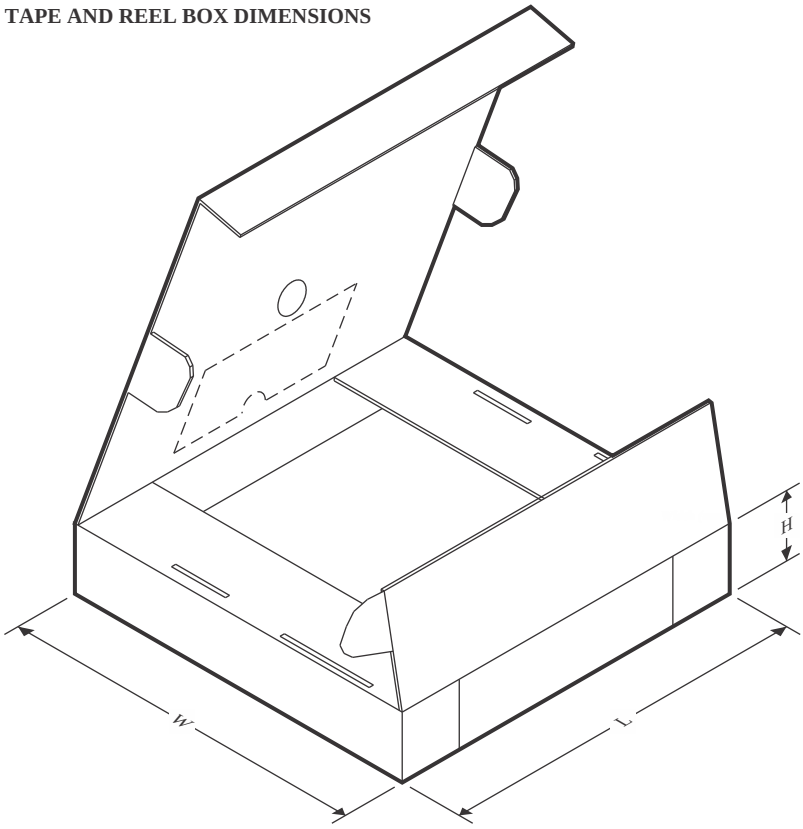
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74201RGRR	VQFN	RGR	20	3000	330.0	12.4	3.8	3.8	1.1	8.0	12.0	Q1
TPS74201RGRT	VQFN	RGR	20	250	180.0	12.5	3.8	3.8	1.1	8.0	12.0	Q1
TPS74201RGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS74201RGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

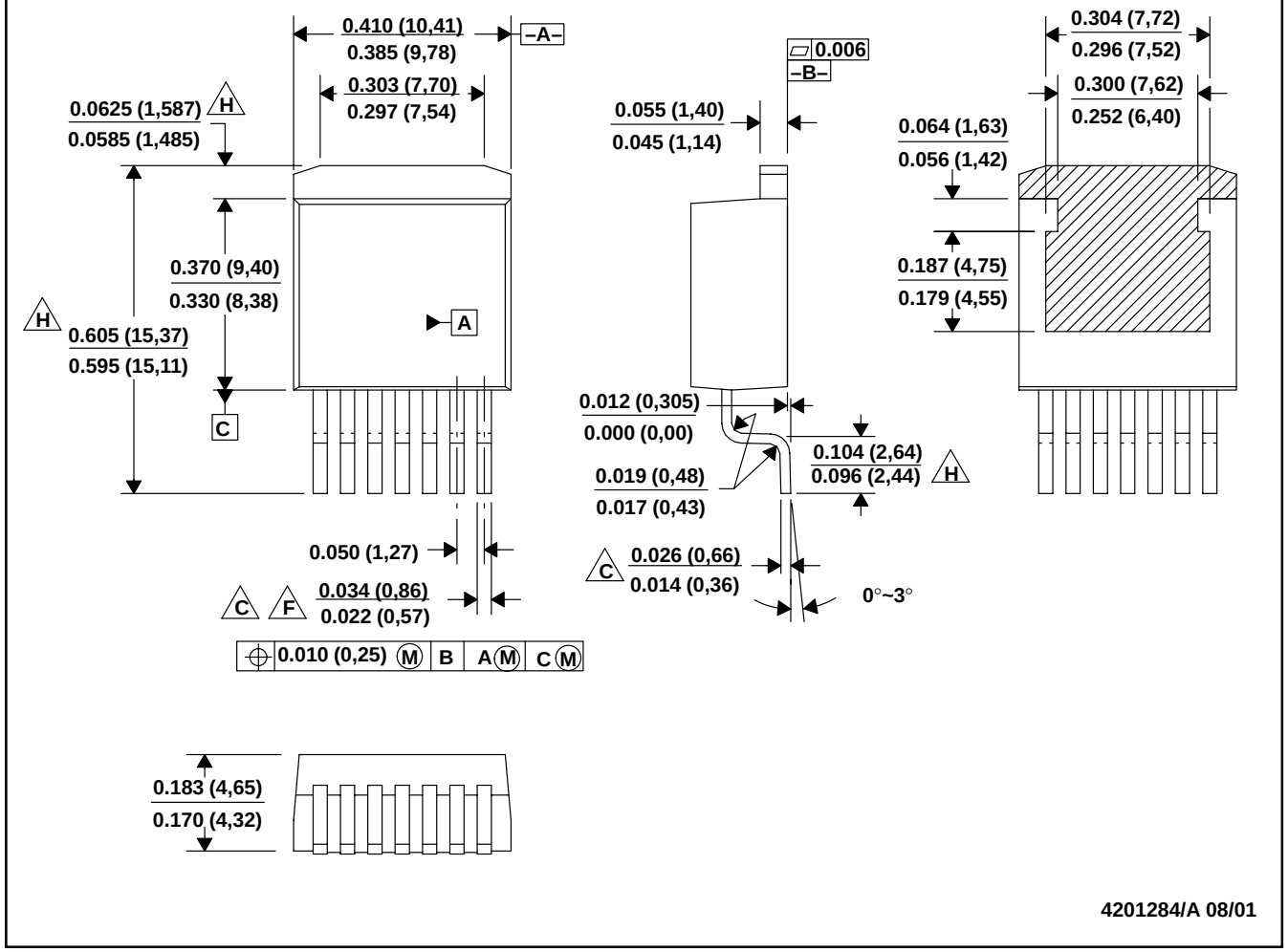
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74201RGRR	VQFN	RGR	20	3000	338.0	355.0	50.0
TPS74201RGRT	VQFN	RGR	20	250	338.0	355.0	50.0
TPS74201RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74201RGWT	VQFN	RGW	20	250	210.0	185.0	35.0

KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

GENERIC PACKAGE VIEW

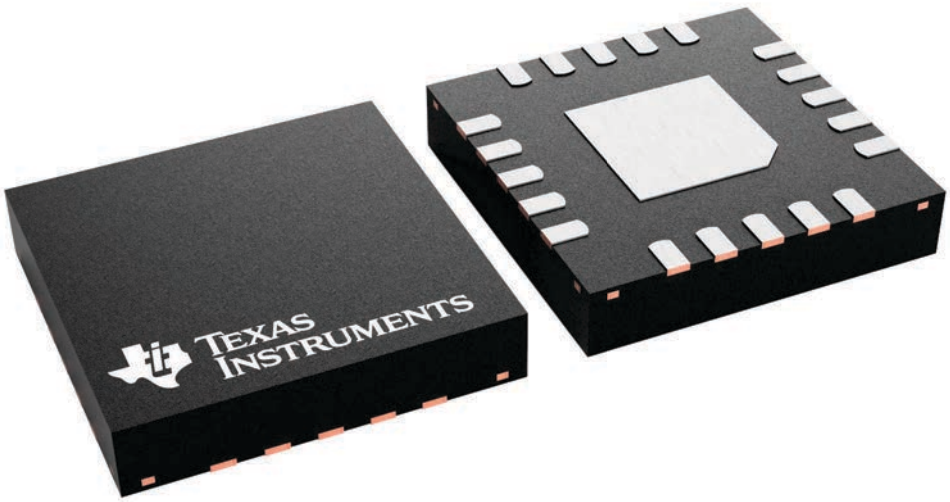
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



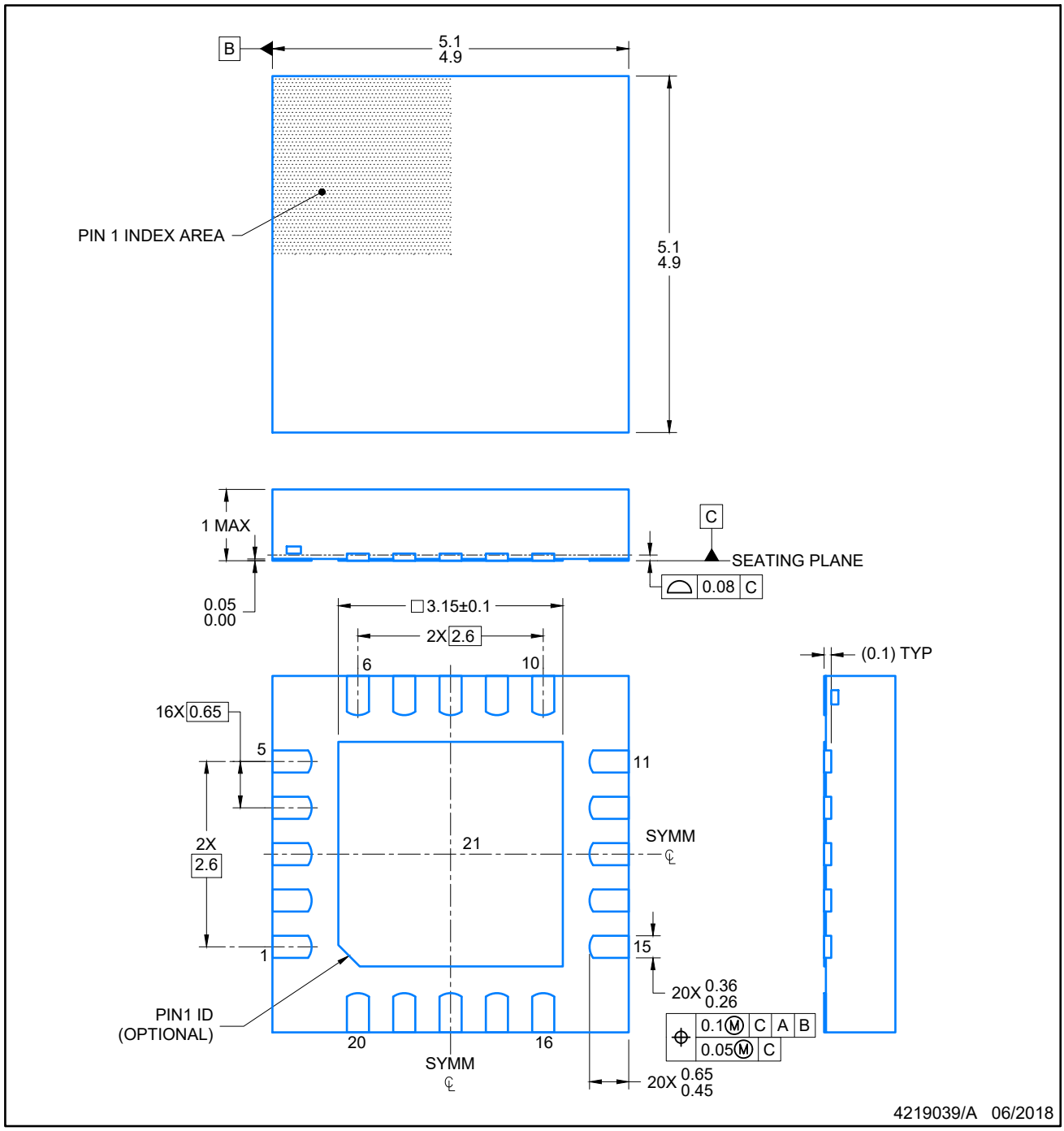
4227157/A

PACKAGE OUTLINE

RGW0020A

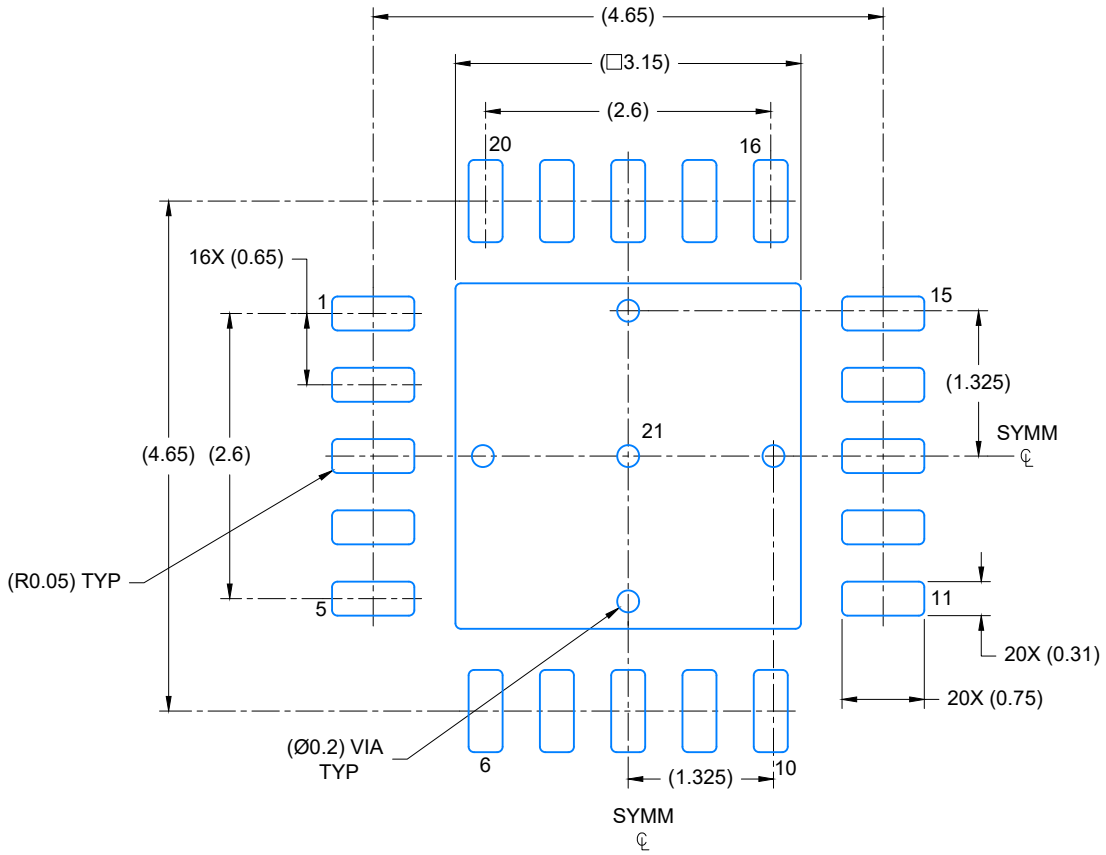
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



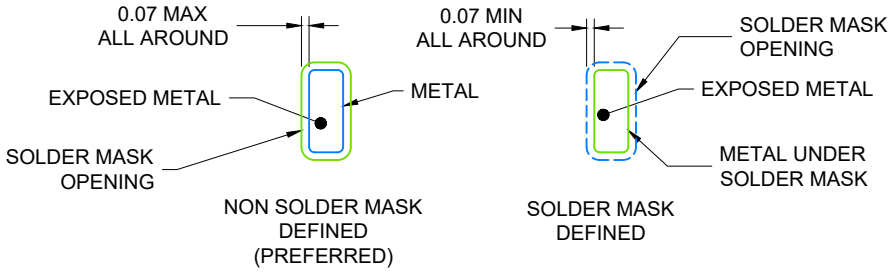
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

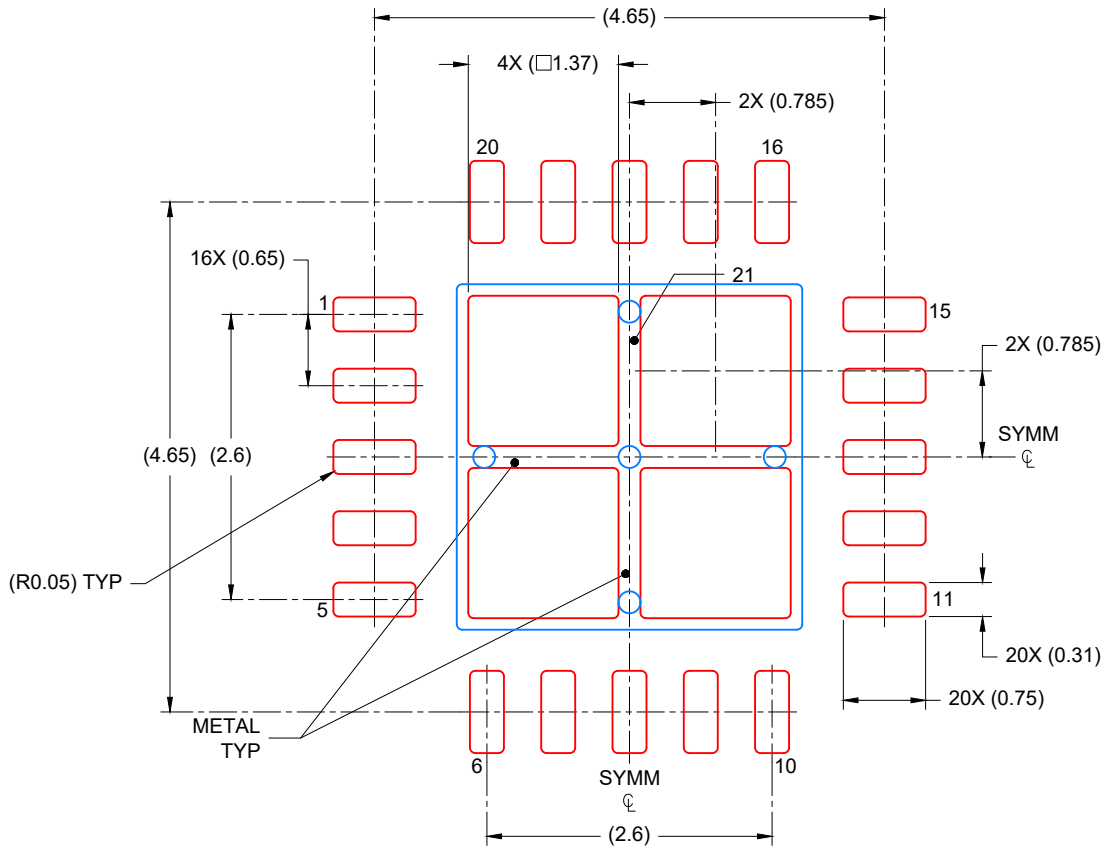


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

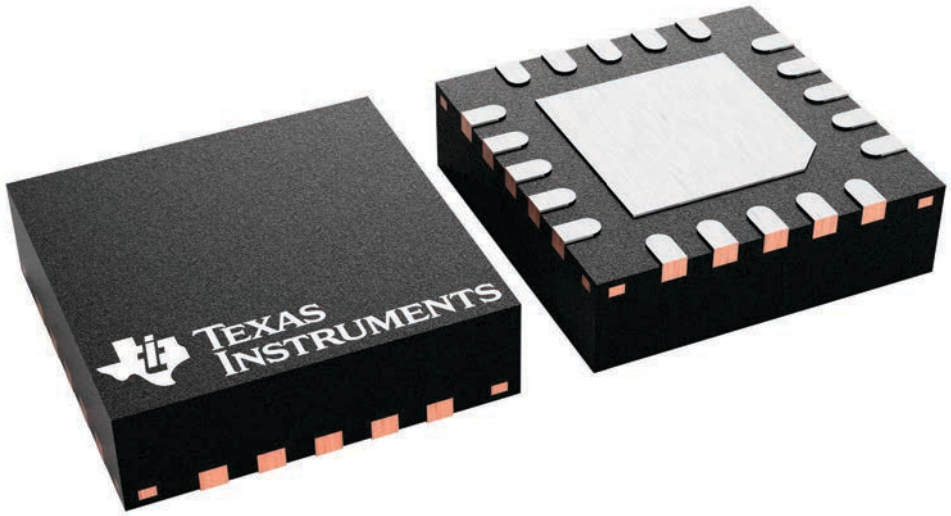
RGR 20

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



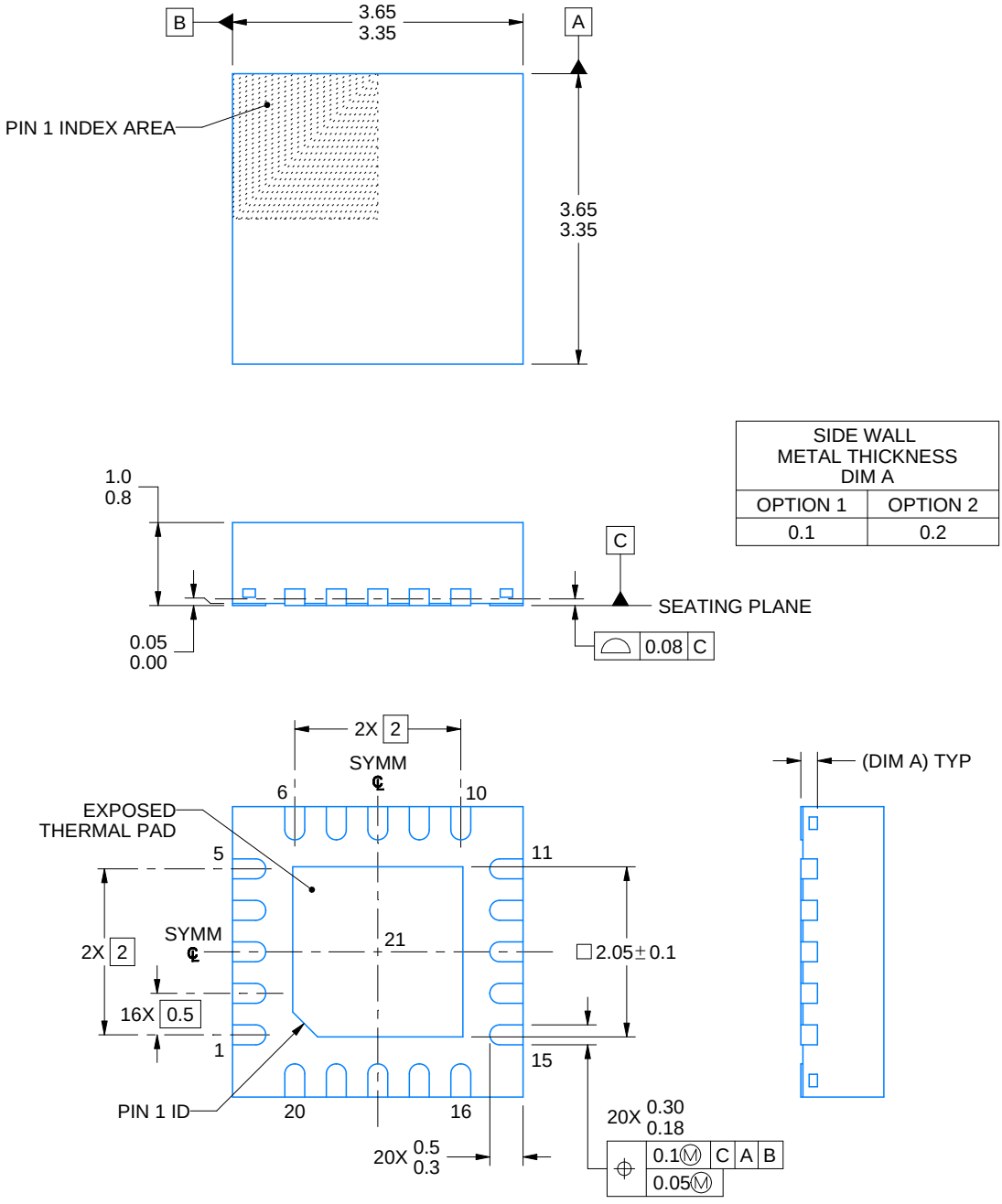
4228482/A

PACKAGE OUTLINE

RGR0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

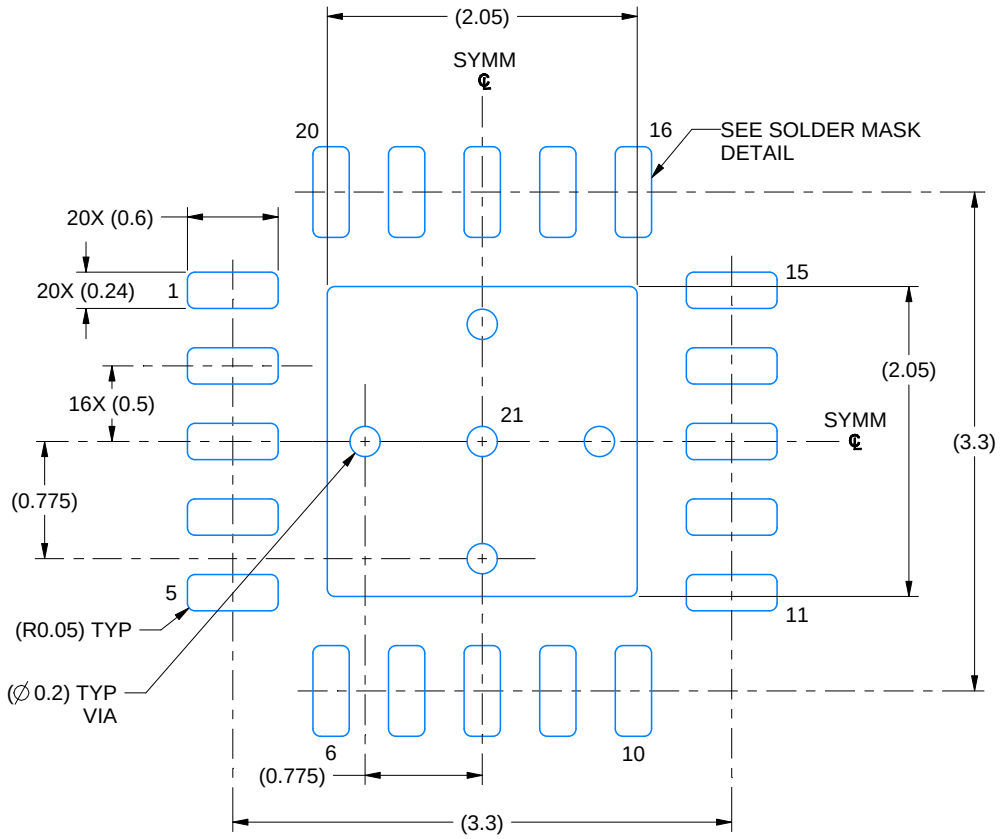


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

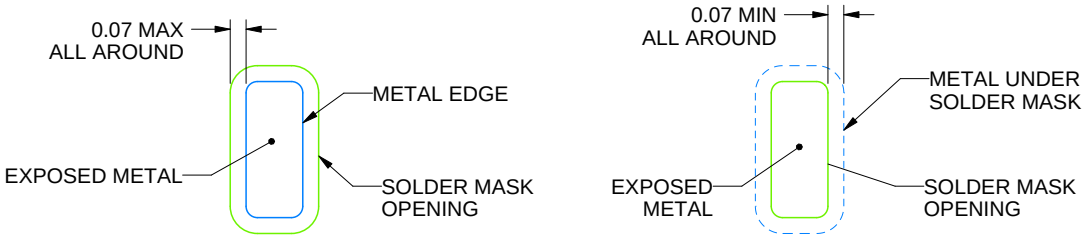
4219031/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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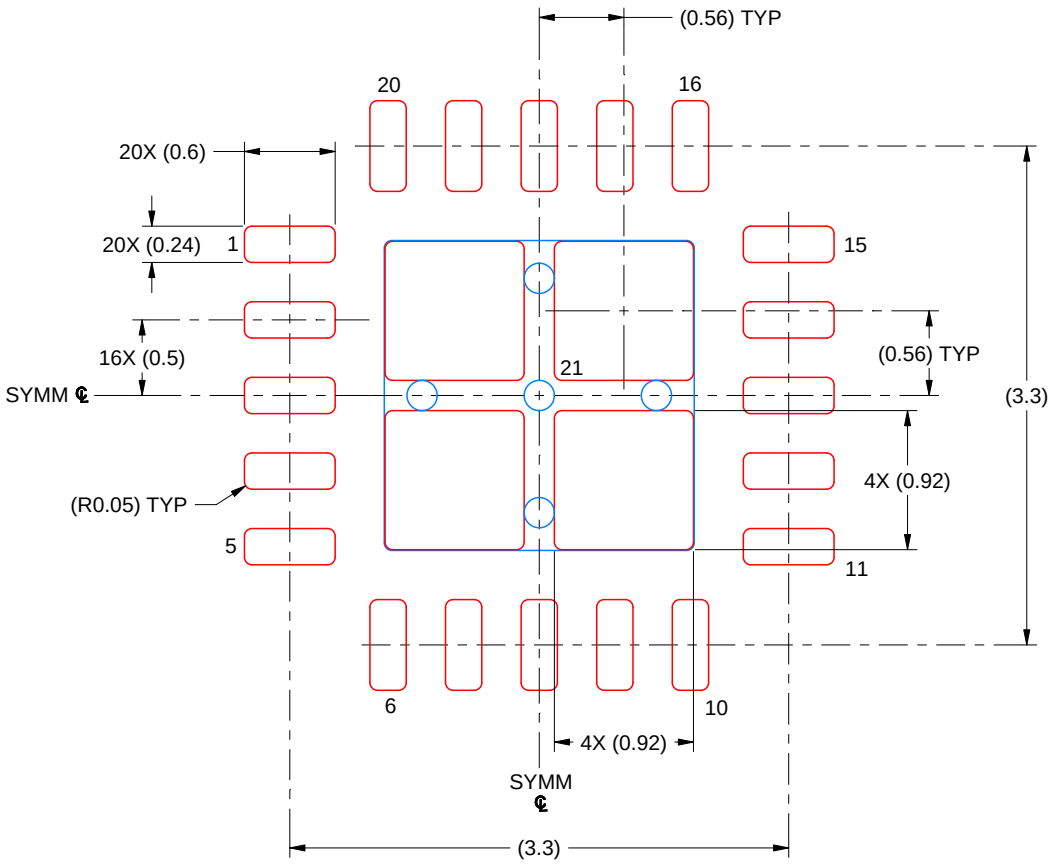
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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