TEXAS INSTRUMENTS
TLV3011, TLV3012, TLV3011B, TLV3012B
JAJSN62C – FEBRUARY 2004 – REVISED APRIL 2023

TLV3011、TLV3012、TLV3011B、TLV3012B 1.24V 基準電圧内蔵低消費電力コンパレータ

1 特長

- 低い静止電流:3.1µA (最大値、「B」バージョン)
- 内蔵基準電圧:1.242V
- 入力同相範囲:レールの 200mV 外まで
- 基準電圧の初期精度:1%
- フェイルセーフ入力 (「B」バージョン)
- パワーオン・リセット (「B」バージョン)
- ヒステリシス内蔵 (「B」バージョン)
- オープン・ドレイン出力オプション (TLV3011x)
- プッシュプル出力オプション (TLV3012x)
- 迅速な応答時間:6µs
- 低い電源電圧:1.65V～5.5V (「B」バージョン)

2 アプリケーション

- 車線離脱警報
- クラスタ
- 有料道路支払い用タグ
- アセット・トラッキング
- バッテリ管理システム

3 概要

TLV3011 は低消費電力オープン・ドレイン出力のコンパレータです。TLV3012 はプッシュプル出力のコンパレータです。どちらのデバイスも、出力先が自由なオンチップ基準電圧を備えており、静止電流は 5µA (最大値) であり、入力同相範囲は電源レールの 200mV 外であり、1.8V～5.5V の単一電源で動作します。内蔵の 1.242V 直列基準電圧は 100ppm/℃以下の低ドリフトを実現しており、最大 10nF の容量性負荷で安定に動作し、最大 0.5mA (標準値) の出力電流を供給できます。

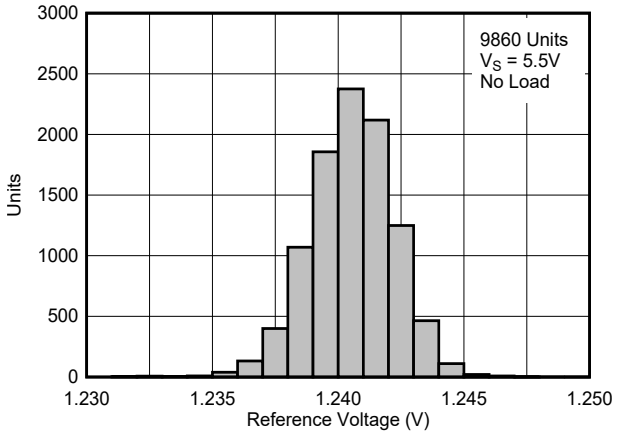
TLV3011B および TLV3012B の「B」バージョンには、パワー・オン・リセット (POR)、フェイルセーフ入力、内蔵ヒステリシスが追加されており、最小電源電圧は 1.65V と低く、最大静止電流は 3.1µA です。

このファミリは、省スペース設計向けの超小型 SOT23-6 パッケージと、基板面積をさらに節約できる SC-70 パッケージで供給されます。どちらのバージョンも、動作温度範囲の仕様は -40℃～+125℃です。

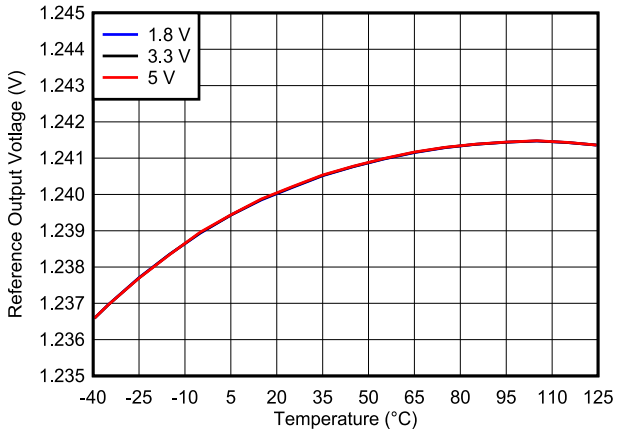
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TLV3011、TLV3012、TLV3011B、TLV3012B	SOT-23 (6)	2.90mm × 1.60mm
	SC-70 (6)	2.00mm × 1.25mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TLV3012B の基準電圧の分布



TLV3012B の基準電圧と温度との関係

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2004) to Revision C (April 2023)	Page
• テキサス・インスツルメンツのフォーマットに変換。「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• 先頭ページのテキストに「B」バージョンを追加。「B」の表とグラフを追加。「B」デバイスのアプリ情報を更新。	1

Changes from Revision A (May 2004) to Revision B (June 2004)	Page
• 先頭ページの不要なピン配置を削除。	1

Changes from Revision * (February 2004) to Revision A (May 2004)	Page
• 「アプリケーション」の一覧を変更	1
• SC-70 パッケージを追加	1
• 不要な注文情報の表を削除、データシートの末尾にある注文情報の付録を参照。	1
• Deleted the *Package Ordering Information* section	3

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5 Pin Configuration and Functions

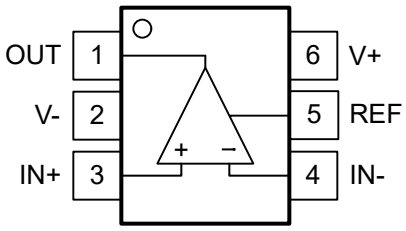

図 5-1. DCK, DBV Package
6-Pin SC-70, SOT-23
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	OUT	O	Comparator Output
2	V–	-	Negative (lowest) power supply
3	IN+	I	Non-inverting comparator input
4	IN–	I	Inverting comparator input
5	REF	O	Reference Output
6	V+	-	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings- TLV3011 and TLV3012

Over operating free-air temperature range (unless otherwise noted)(1).

			MIN	MAX	UNIT
	Supply voltage			7	V
	Signal input pins	Voltage(2)	–0.5	(V+) +0.5	V
		Current(2)		±10	mA
	Output short circuit(3)		Continuous		
	Operating temperature		–40	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin.
(3) Short circuit to ground

6.2 Absolute Maximum Ratings - TLV3011B and TLV3012B

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.5	7	V
Input pins (IN+, IN–) from (V–)(2)	–0.5	7	V
Output (OUT) (Open-Drain) from (V–)(3)	–0.5	7	V
Output (OUT) (Push-Pull) from (V–)	–0.5	(V+) + 0.5	V
Output short circuit current(4)		10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to (V–). Inputs (IN+, IN–) can be greater than (V+) as long as within the –0.5 V to 7 V range. Inputs beyond –0.3 V must be current-limited to less than –10 mA, while inputs beyond 7 V must be externally voltage clamped.
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as it is within the –0.5 V to 7 V range
(4) Short-circuit to (V–) or (V+).

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

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6.4 Thermal Information - TLV3011 and TLV3012

THERMAL METRIC[1]		TLV3011, TLV3012		UNIT
		DCK (SC-70)	DBV (SOT-23)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.4	191.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	141.3	123.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.2	38.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	53.6	21.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.0	38.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information- TLV3011B and TLV3012B

THERMAL METRIC[1]		TLV3011B, TLV3012B		UNIT
		DCK (SC-70)	DBV (SOT-23)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	169.8	162.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.5	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.2	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.9	21.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.0	41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.6 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)		1.8	5.5	V
Supply voltage: V_S = (V+) – (V–)	B-Versions	1.65	5.5	V
Input voltage range from (V–)		–0.2	(V+) + 0.2	V
Output voltage range from (V–) for open drain		–0.2	(V+)	V
Output voltage range from (V–) for open drain	B-Versions	–0.2	5.5	V
Ambient temperature, T_A		–40	125	°C

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6.7 Electrical Characteristics - TLV3011 and TLV3012

V_S = 1.8 V to 5.5 V, at T_A = 25°C, V_{OUT} = V_S, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = 0 V, I_O = 0 V		0.5	15	mV
dV_{OS}/dT	Input offset voltage vs temperature	T_A = –40°C to +125°C		±12		µV/°C
PSRR	Power supply rejection ratio	V_S = 1.8 V to 5.5 V		100	1000	µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		±10		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		±10		pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = –0.2 V to (V+) – 1.5 V	60	74		dB
		V_{CM} = –0.2 V to (V+) + 0.2 V	54	62		
INPUT IMPEDANCE						
	Common mode			10^{13} ‖ 2		Ω ‖ pF
	Differential			10^{13} ‖ 4		Ω ‖ pF
OUTPUT						
V_{OL}	Voltage output low from rail	V_S = 5 V, I_{OUT} = –5 mA		160	200	mV
V_{OH}	Voltage output high from rail	V_S = 5 V, I_{OUT} = 5 mA		90	200	mV
	Short-circuit current				See Typical Characteristics	
VOLTAGE REFERENCE						
V_{OUT}	Output voltage		1.208	1.242	1.276	V
	Initial accuracy				±1%	
dV_{OUT}/d_T	Temperature drift	–40°C ≤ T_A ≤ 125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load regulation, sourcing	0 mA < I_{SOURCE} ≤ 0.5 mA		0.36	1	mV/mA
	Load regulation, sinking	0 mA < I_{SINK} ≤ 0.5 mA		6.6		
I_{LOAD}	Output current			0.5		mA
dV_{OUT}/dV_{IN}	Line regulation	1.8 V ≤ V_{IN} ≤ 5.5 V		10	100	µV/V
NOISE						
	Reference voltage noise	f = 0.1 Hz to 10 Hz		0.2		mV_{PP}
POWER SUPPLY						
V_S	Specified voltage		1.8		5.5	V
	Operating voltage range		1.8		5.5	V
I_Q	Quiescent current	V_S = 5 V, V_O = High		2.8	5	µA
TEMPERATURE						
	Operating range		–40		125	°C
	Storage range		–65		150	°C

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6.8 Switching Characteristics - TLV3011 and TLV3012

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Propagation delay time, low to high	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		12		µs
		f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6		
	Propagation delay time, high to low	f = 10 kHz, V_{STEP} = 1 V, input overdrive = 10 mV		13.5		µs
		f = 10 kHz, V_{STEP} = 1 V, input overdrive = 100 mV		6.5		
t_r	Rise time	C_L = 10 pF		100		ns
t_f	Fall time	C_L = 10 pF		100		ns

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6.9 Electrical Characteristics - TLV3011B and TLV3012B

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = (V–)	–6	±0.3	6	mV
V_{OS}	Input offset voltage	V_{CM} = (V–) T_A = –40°C to +125°C	–9		9	mV
dV_{IO}/dT	Input offset voltage drift	V_{CM} = (V–) T_A = –40°C to +125°C		±12		µV/°C
PSRR	power supply rejection ratio	V_{CM} = (V–) V_S = 1.65 V to 5.5 V T_A = –40°C to +125°C		100	1000	µV/V
V_{HYS}	Input hysteresis voltage	T_A = –40°C to +125°C	2	6	8	mV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S /2	–10((1))	±4.5	10((1))	pA
I_{OS}	Input offset current	V_{CM} = V_S /2	–10((1))	±1	10((1))	pA
INPUT COMMON MODE RANGE						
$V_{CM-Range}$	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common mode rejection ratio	V_{CM} = (V–) + 1.5V to (V+) + 0.2V V_S = 5.5 V	60	74		dB
CMRR	Common mode rejection ratio	V_{CM} = (V–) - 0.2V to (V+) + 0.2V V_S = 5.5 V	54	62		dB
R_{CM}	Input Common Mode Resistance			10^{13}		Ω
C_{IC}	Input Common Mode Capacitance			2		pF
INPUT IMPEDANCE						
R_{DM}	Input Differential Mode Resistance			10^{13}		Ω
C_{ID}	Input Differential Mode Capacitance			4		pF
OUTPUT						
V_{OL}	Voltage swing from (V–)	V_S = 5 V I_{SINK} = 5 mA T_A = –40°C to +125°C		160	200	mV
V_{OH}	Voltage swing from (V+) (for Push-Pull only)	V_S = 5 V I_{SOURCE} = 5 mA T_A = –40°C to +125°C		90	200	mV
VOLTAGE REFERENCE						
V_{OUT}	Reference Voltage		1.223	1.242	1.260	V
	Accuracy			±0.25%	±1.5%	
dV_{OUT}/d_T	Temperature Drift	T_A = –40°C to +125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load Regulation, Sourcing	0 mA < I_{SOURCE} ≤ 0.5 mA		0.36	1((1))	mV/mA
	Load Regulation, Sinking	0 mA < I_{SINK} ≤ 0.5 mA		6.6		mV/mA
ILOAD	Output Current			0.5		mA
dV_{OUT}/dV_S	Line Regulation	1.65 V ≤ V_S ≤ 5.5 V		10	100((1))	µV/V
V_{noise}	Noise	f = 0.1 Hz to 10 Hz		0.2		mV_{PP}

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6.9 Electrical Characteristics - TLV3011B and TLV3012B (continued)

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8V and 5.5V, V_{CM} = V_S /2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per comparator	Output is logic high		2.4	3.1	µA
I_Q	Quiescent current per comparator	Output is logic high T_A = –40°C to +125°C			3.6	µA

(1) Ensured by characterization

6.10 Switching Characteristics - TLV3011B and TLV3012B

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 1.8 V and 5.5 V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-LH}	Propagation delay time, low-to-high (push-pull output)	f = 10 kHz, V_{STEP} = 200mV, V_{OD} = 100 mV, C_L = 10 pF		2	4	µs
T_{PD-HL}	Propagation delay time, high-to-low	f = 10 kHz, V_{STEP} = 200mV, V_{OD} = 100 mV, C_L = 10 pF		2	4	µs
T_{RISE}	Output Rise Time, 20% to 80%, push-pull output	C_L = 10 pF		10		ns
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 10 pF		10		ns
T_{FALL}	Output Fall Time, 80% to 20%, open-drain output	R_L = 10 kΩ, C_L = 10 pF		10		ns
t_{ON}	Power on-time			1.9		ms

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7 Typical Characteristics - TLV3011 and TLV3012

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

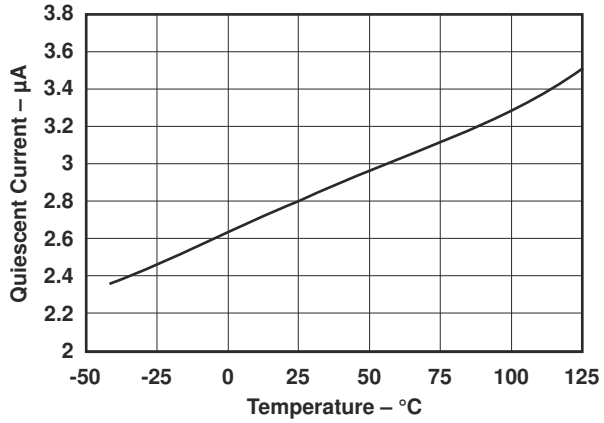

図 7-1. Quiescent Current vs Temperature

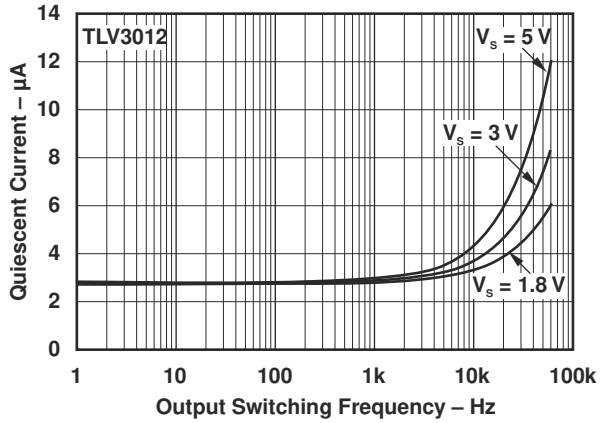

図 7-2. Quiescent Current vs Output Switching Frequency

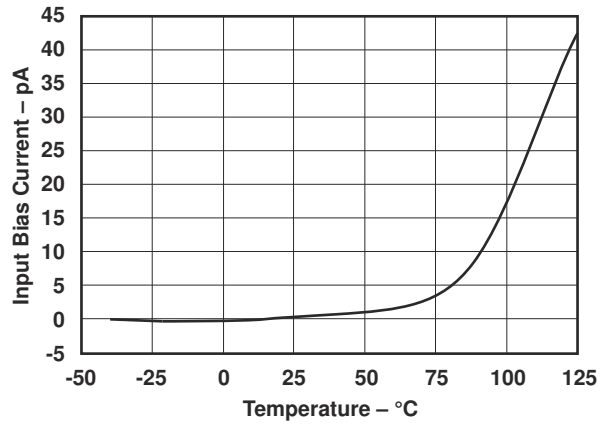

図 7-3. Input Bias Current vs Temperature

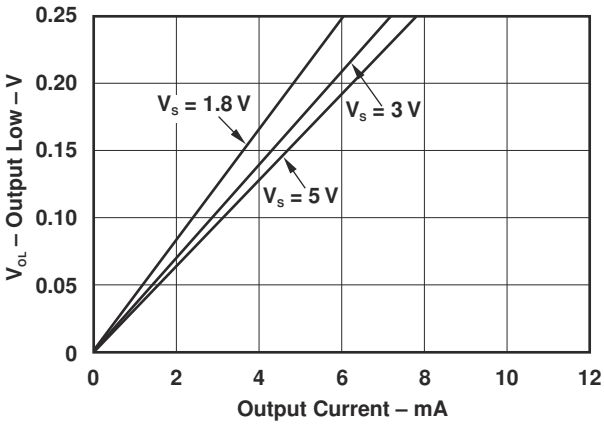

図 7-4. Output Low vs Output Current

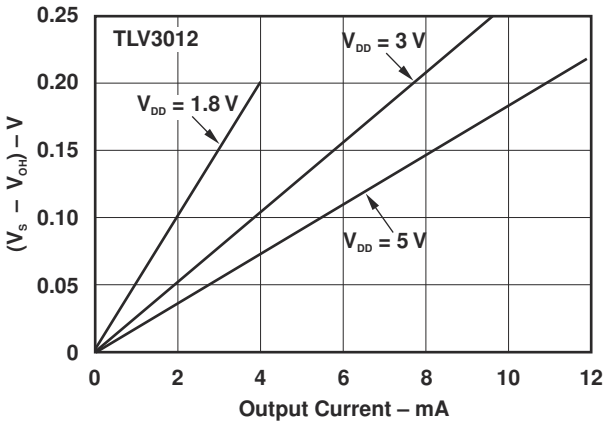

図 7-5. Output High vs Output Current

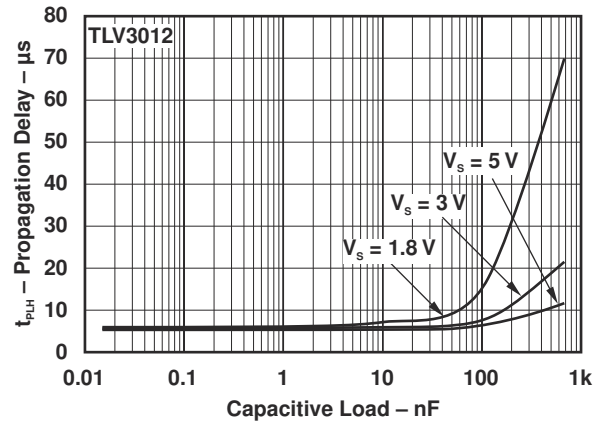

図 7-6. Propagation Delay (t_{PLH}) vs Capacitive Load

7 Typical Characteristics - TLV3011 and TLV3012 (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

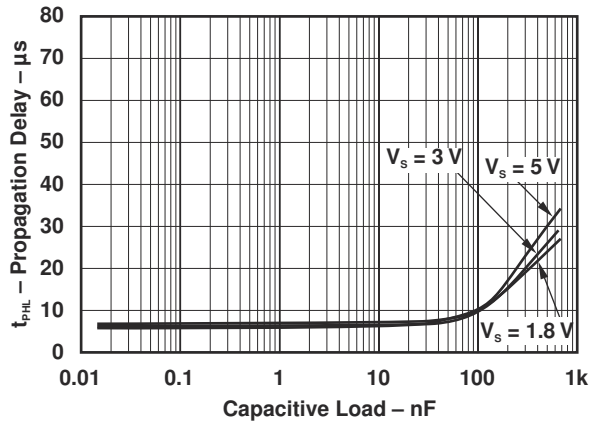

図 7-7. Propagation Delay (t_{PHL}) vs Capacitive Load

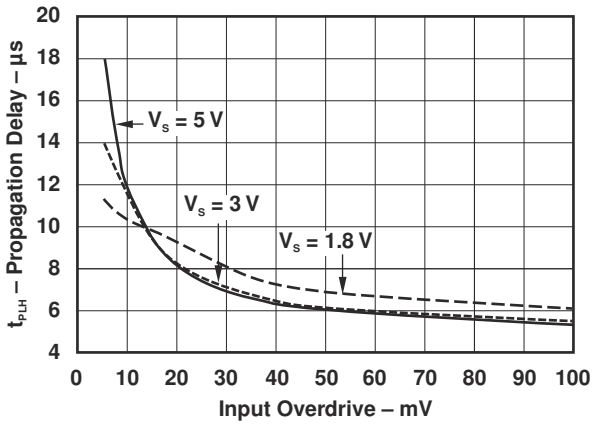

図 7-8. Propagation Delay (t_{PLH}) vs Input Overdrive

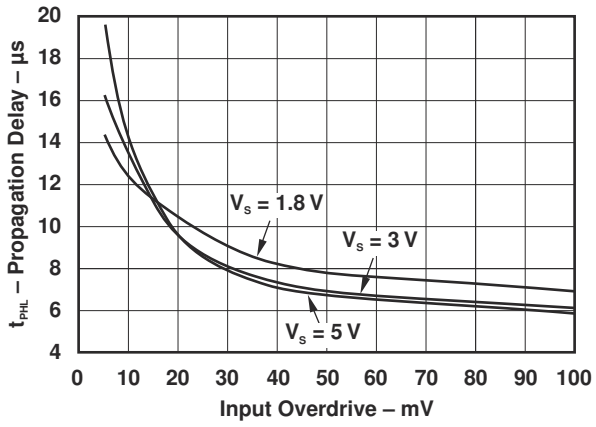

図 7-9. Propagation Delay (t_{PHL}) vs Input Overdrive

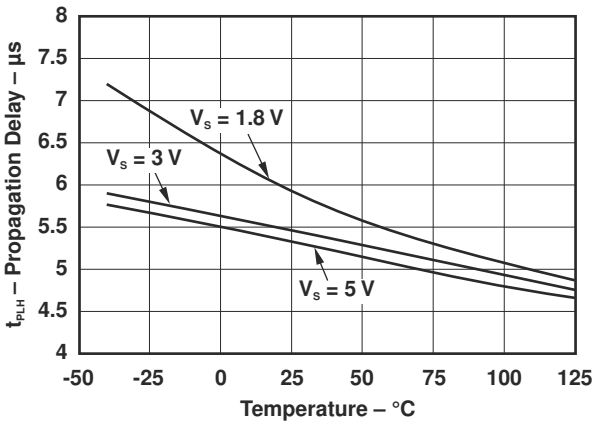

図 7-10. Propagation Delay (t_{PLH}) vs Temperature

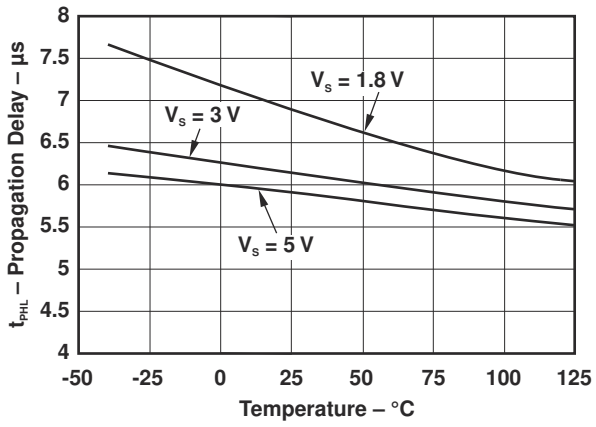

図 7-11. Propagation Delay (t_{PHL}) vs Temperature

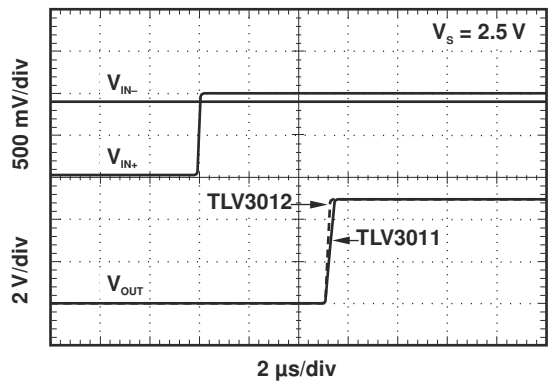

図 7-12. Propagation Delay (t_{PLH})

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7 Typical Characteristics - TLV3011 and TLV3012 (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

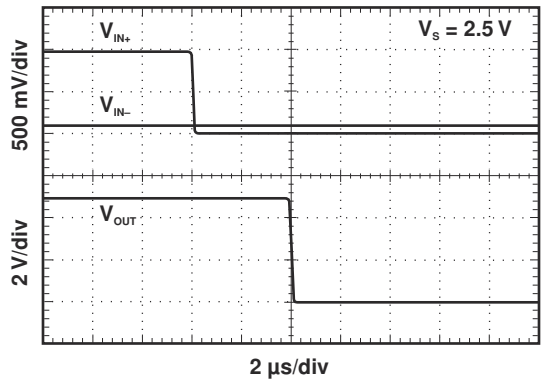

図 7-13. Propagation Delay (t_{PHL})

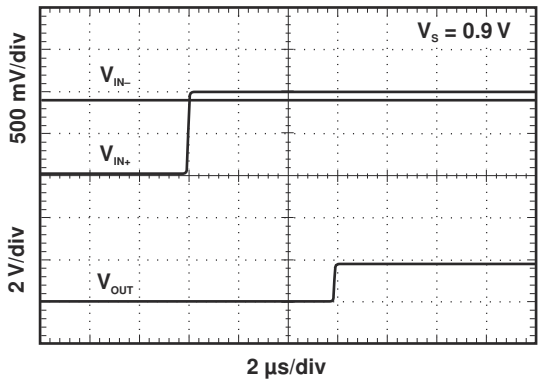

図 7-14. Propagation Delay (t_{PLH})

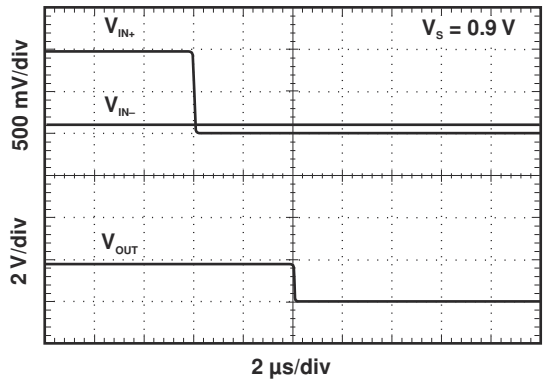

図 7-15. Propagation Delay (t_{PHL})

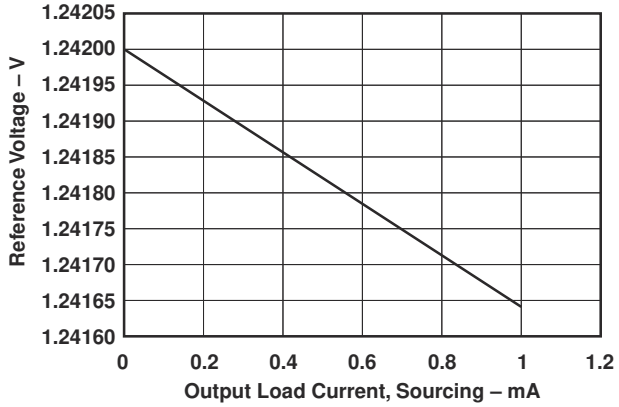

図 7-16. Reference Voltage vs Output Load Current (Sourcing)

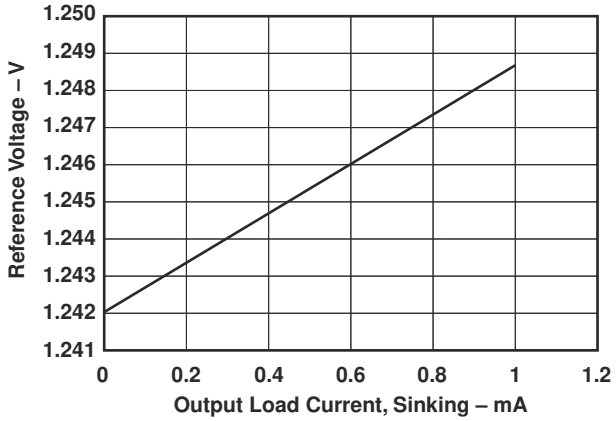

図 7-17. Reference Voltage vs Output Load Current (Sinking)

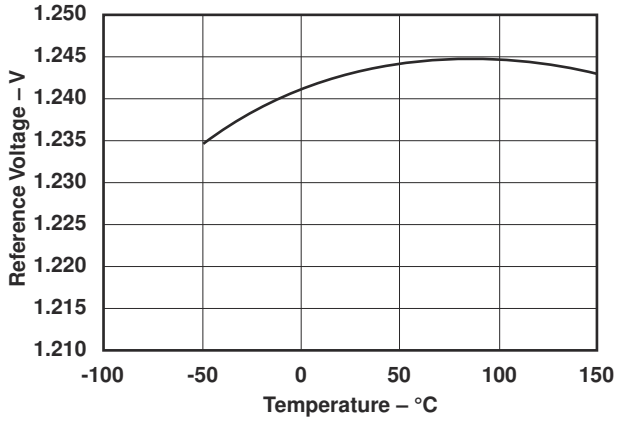

図 7-18. Reference Voltage vs Temperature

7 Typical Characteristics - TLV3011 and TLV3012 (continued)

At T_A = 25°C, V_S = 1.8 V to 5.5 V, and Input Overdrive = 100 mV, unless otherwise noted.

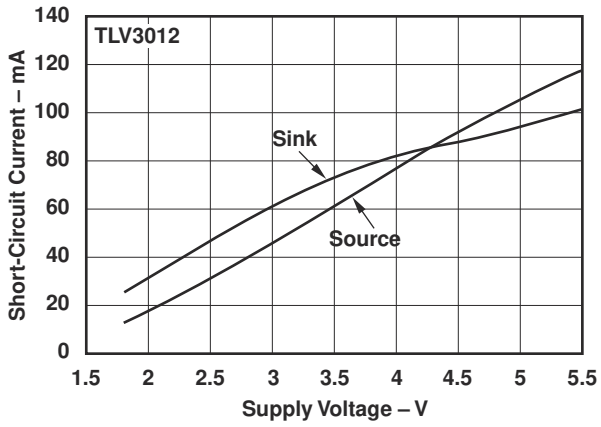

図 7-19. Short-Circuit Current vs Supply Voltage

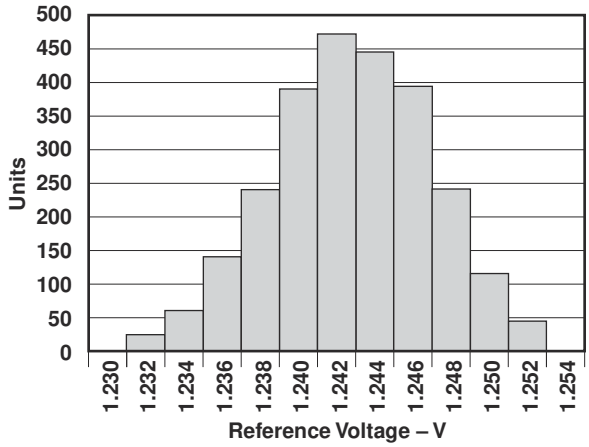

図 7-20. Reference Voltage Distribution

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8 Typical Characteristics - TLV3011B and TLV3012B

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

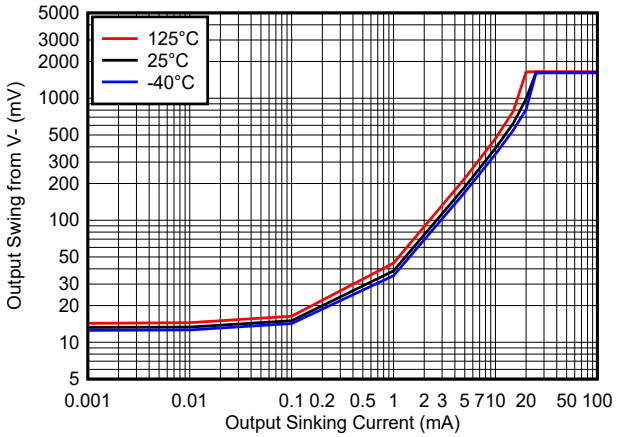

図 8-1. Output Swing vs. Output Sinking Current - 1.8V

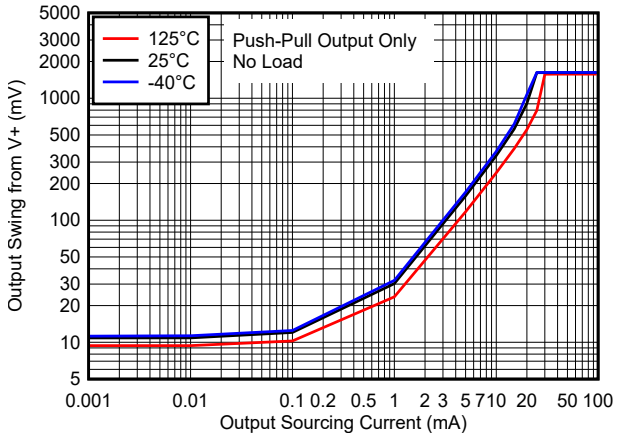

図 8-2. Output Swing vs. Output Sourcing Current - 1.8V

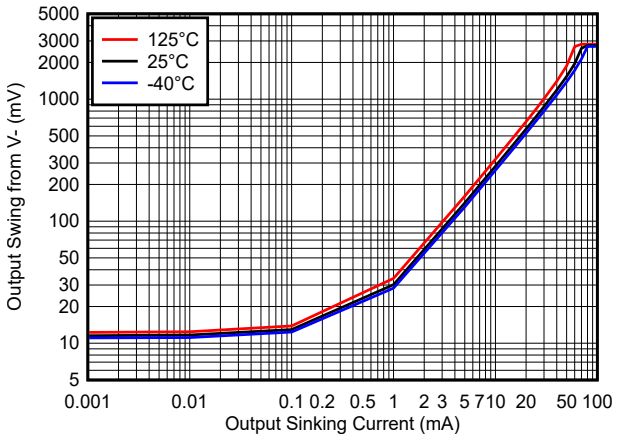

図 8-3. Output Swing vs. Output Sinking Current - 3.3V

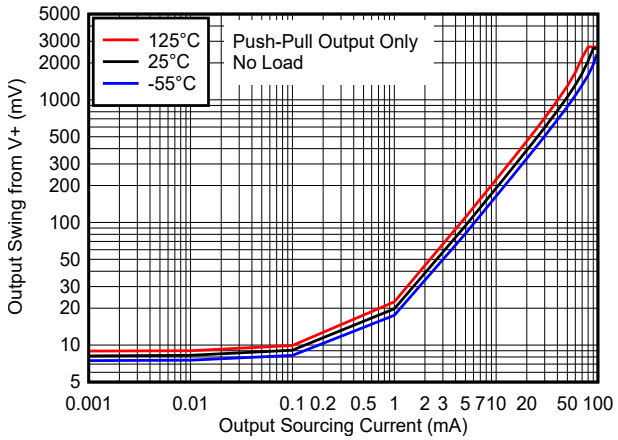

図 8-4. Output Swing vs. Output Sourcing Current - 3.3V

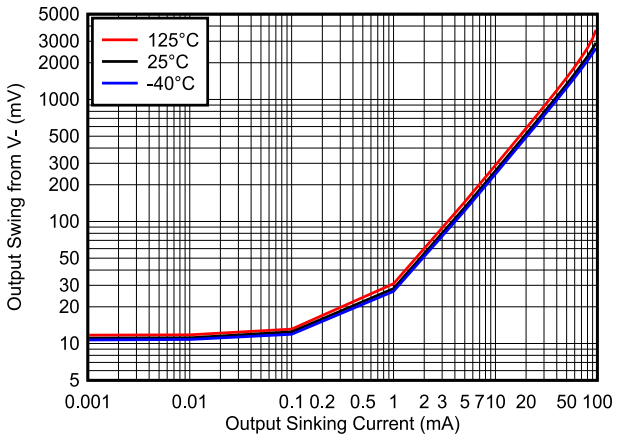

図 8-5. Output Swing vs. Output Sinking Current - 5V

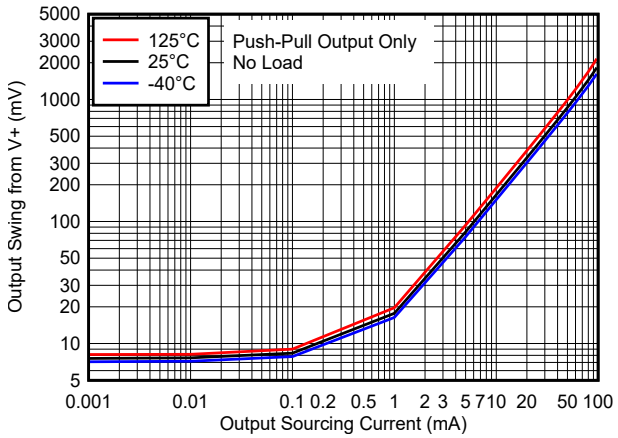

図 8-6. Output Swing vs. Output Sourcing Current - 5V

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8 Typical Characteristics - TLV3011B and TLV3012B (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

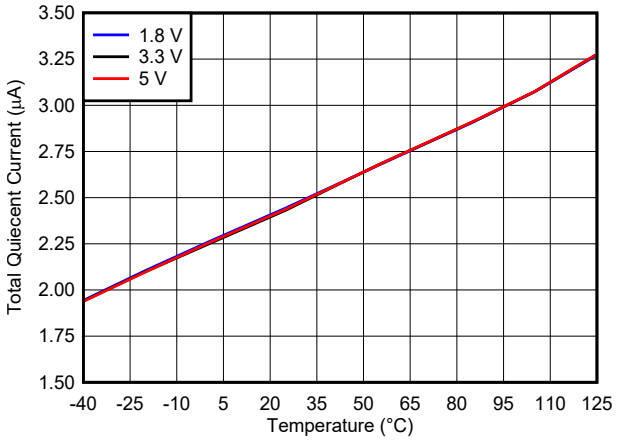

図 8-7. Supply Current vs. Temperature

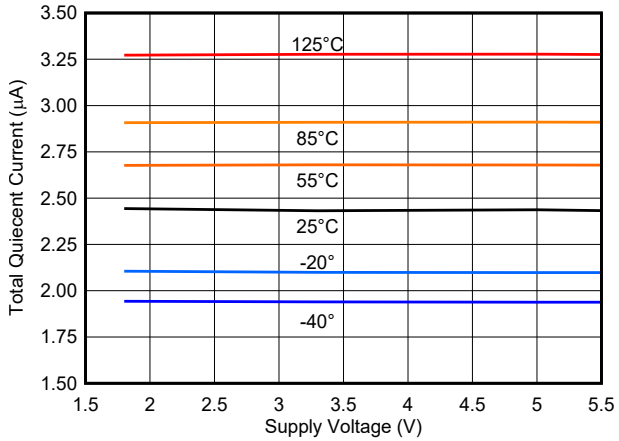

図 8-8. Supply Current vs. Supply Voltage

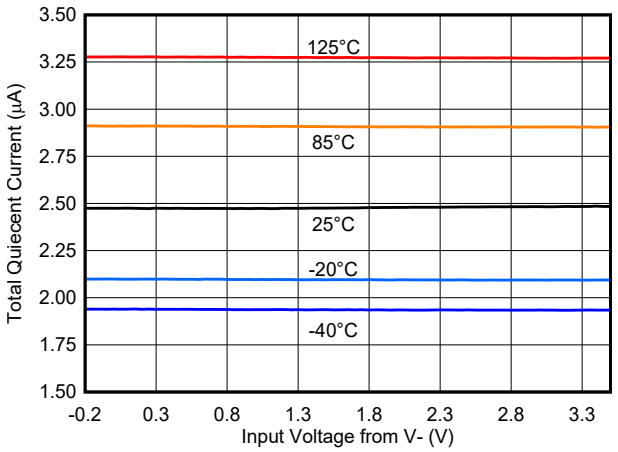

図 8-9. Supply Current vs. Common Mode - 3.3V

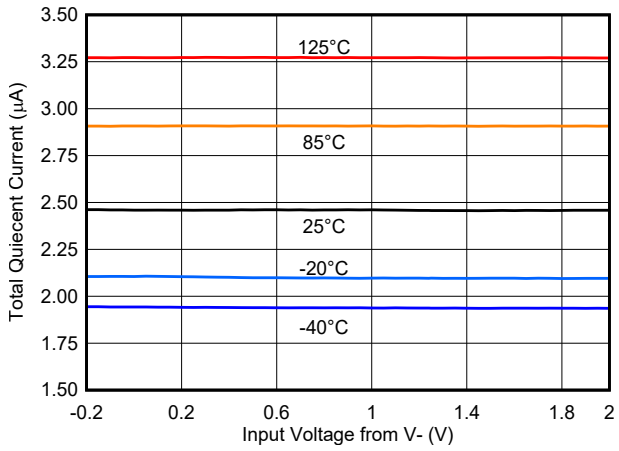

図 8-10. Supply Current vs. Common Mode - 1.8V

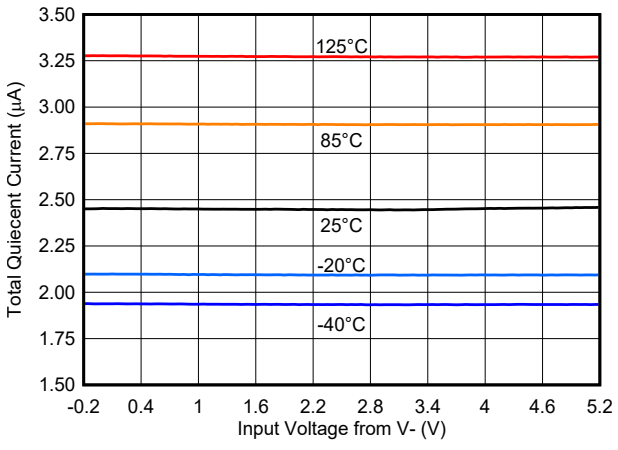

図 8-11. Supply Current vs. Common Mode - 5V

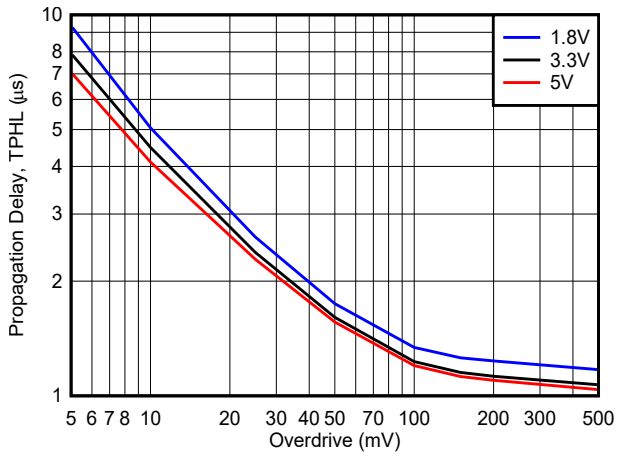

図 8-12. High to Low Propagation Delay vs. Overdrive

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8 Typical Characteristics - TLV3011B and TLV3012B (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

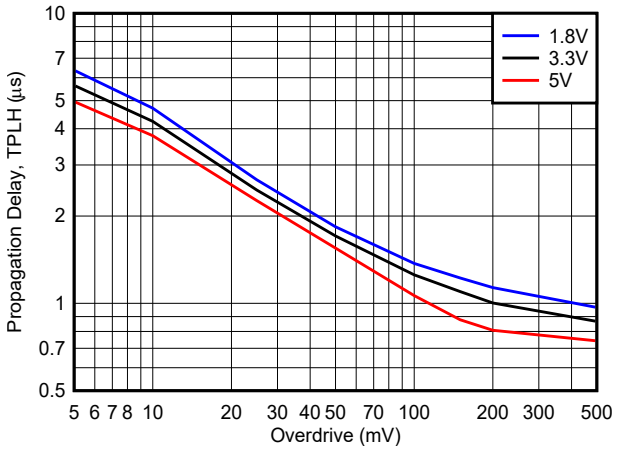

図 8-13. Low to High Propagation Delay vs. Overdrive

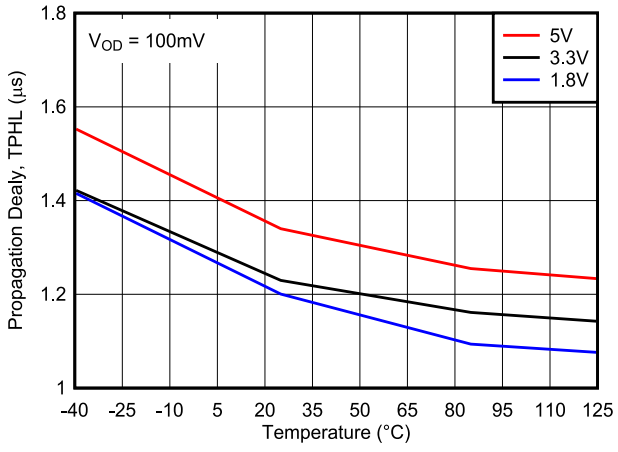

図 8-14. High to Low Propagation Delay vs. Temperature

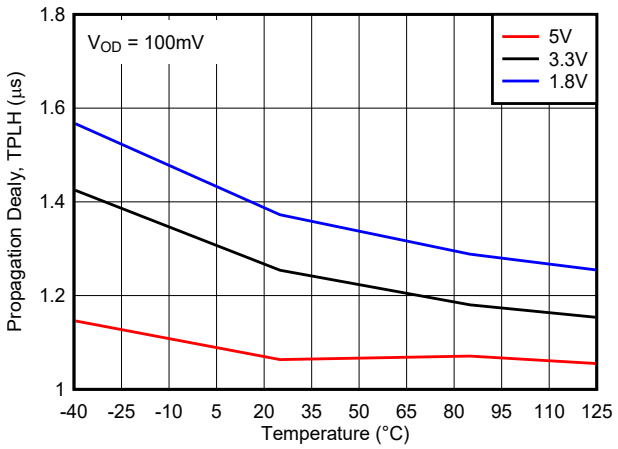

図 8-15. Low to High Propagation Delay vs. Temperature

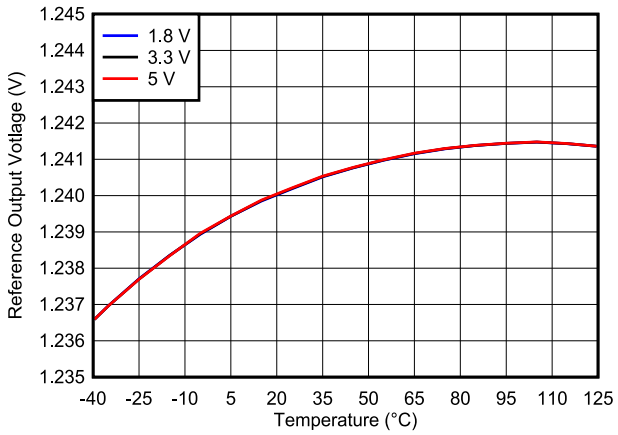

図 8-16. Reference Voltage vs. Temperature

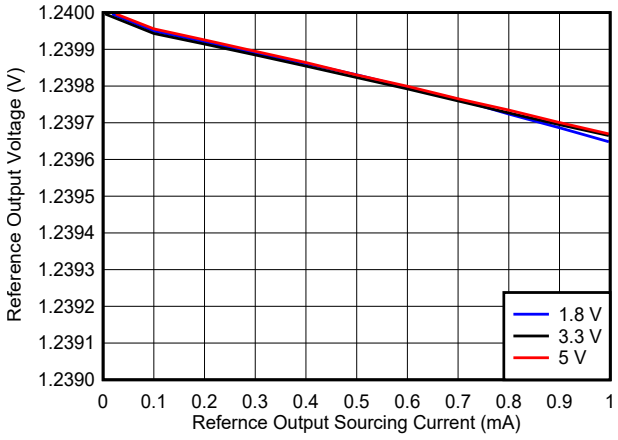

図 8-17. Reference Voltage vs. Reference Output Sourcing Current

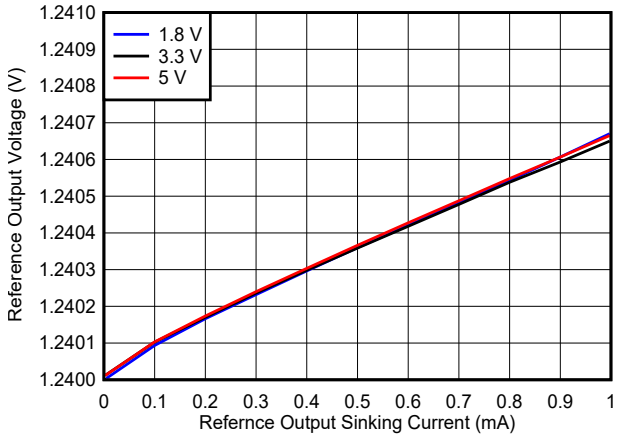

図 8-18. Reference Voltage vs. Reference Output Sinking Current

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8 Typical Characteristics - TLV3011B and TLV3012B (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

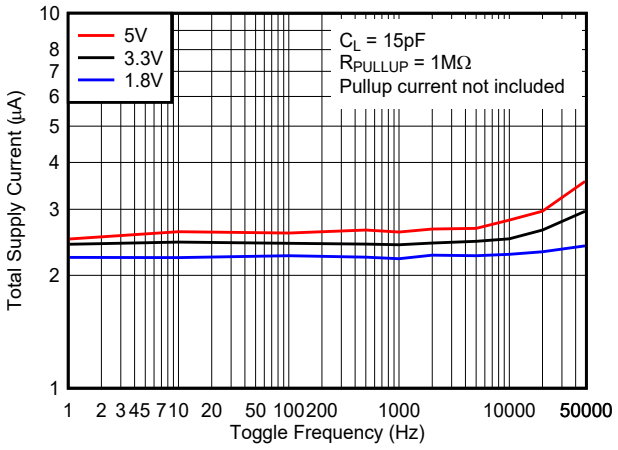

図 8-19. Supply Current vs. Toggle Frequency - Open Drain Output

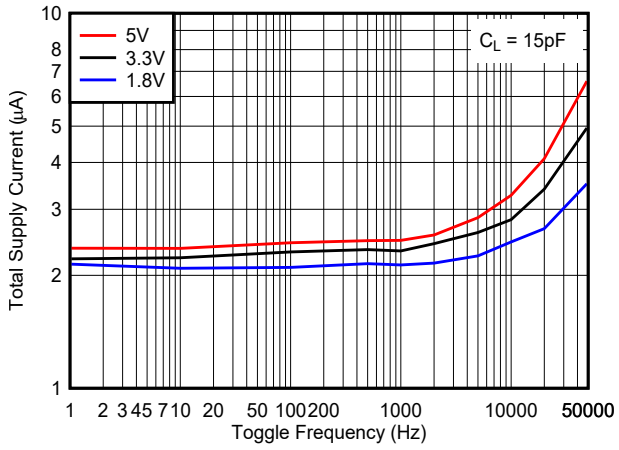

図 8-20. Supply Current vs. Toggle Frequency - Push-Pull Output

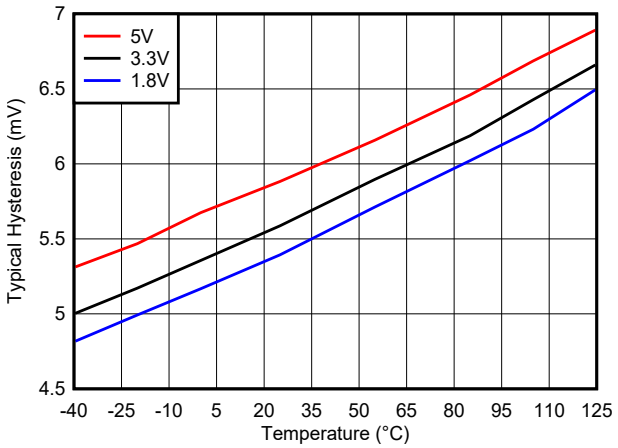

図 8-21. Hysteresis Voltage vs. Temperature

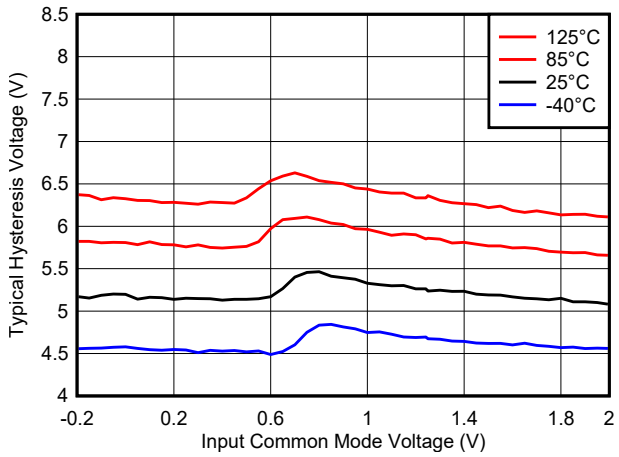

図 8-22. Hysteresis Voltage vs. Common Mode, 1.8V

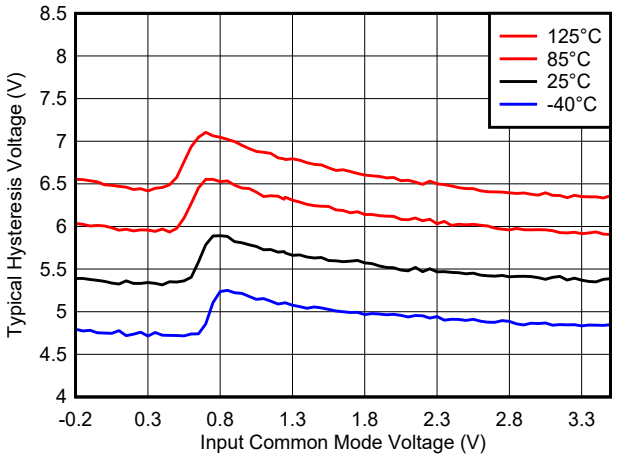

図 8-23. Hysteresis Voltage vs. Common Mode, 3.3V

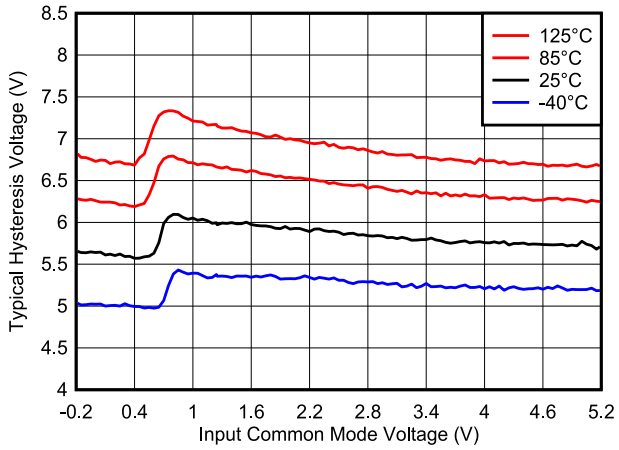

図 8-24. Hysteresis Voltage vs. Common Mode, 5V

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8 Typical Characteristics - TLV3011B and TLV3012B (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

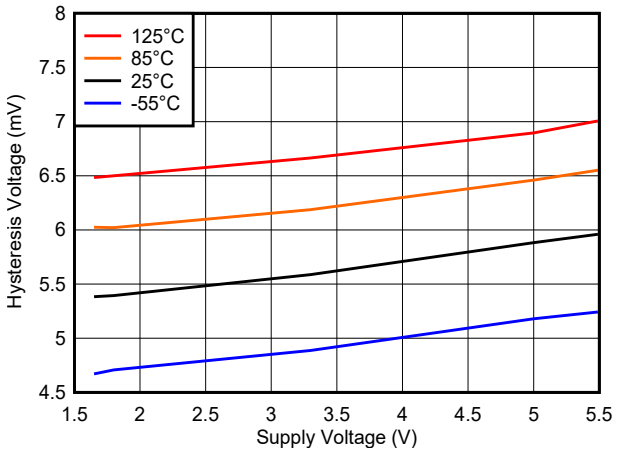

図 8-25. Hysteresis Voltage vs. Supply Voltage

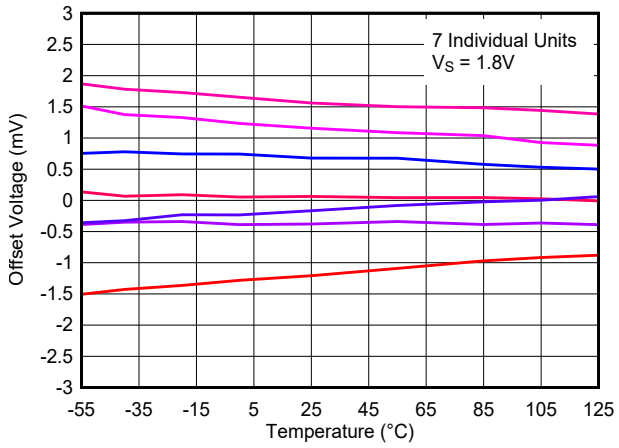

図 8-26. Offset Voltage vs. Temperature, 1.8 V

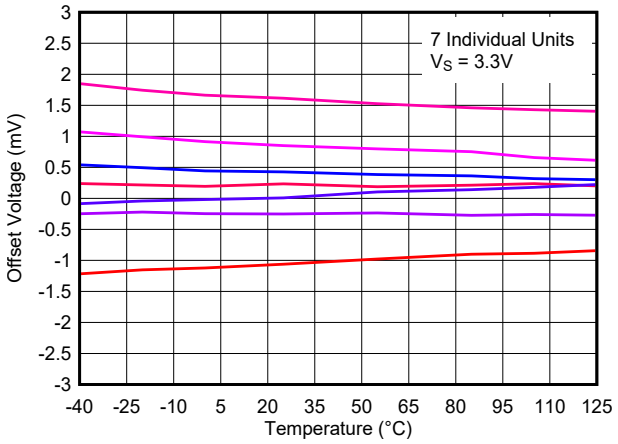

図 8-27. Offset Voltage vs. Temperature, 3.3 V

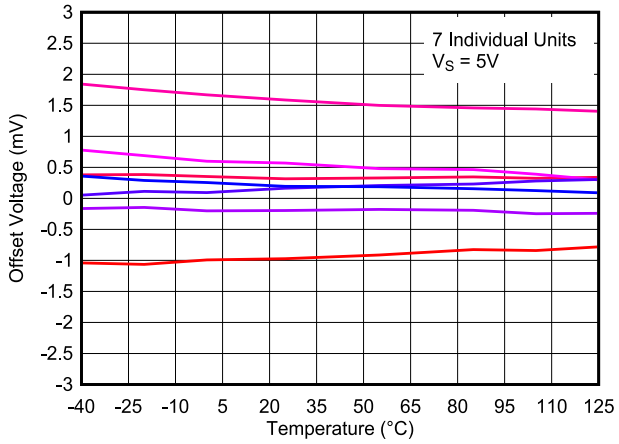

図 8-28. Offset Voltage vs. Temperature, 5 V

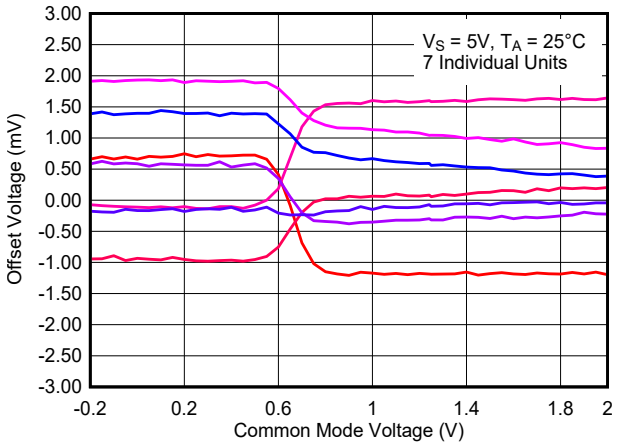

図 8-29. Offset Voltage vs. Common Mode Voltage, 1.8 V

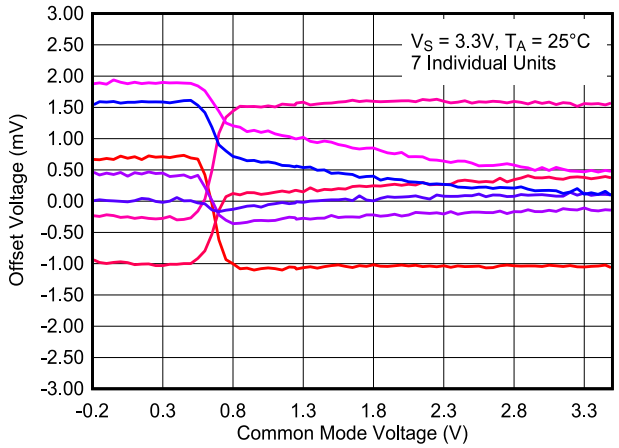

図 8-30. Offset Voltage vs. Common Mode Voltage, 3.3 V

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8 Typical Characteristics - TLV3011B and TLV3012B (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = +5V, V_{CM} = V_S /2 at T_A = 25°C , R_{PULLUP} = 1MΩ to V+, C_L = 15pF, V_{OD} = 100mV unless otherwise noted.

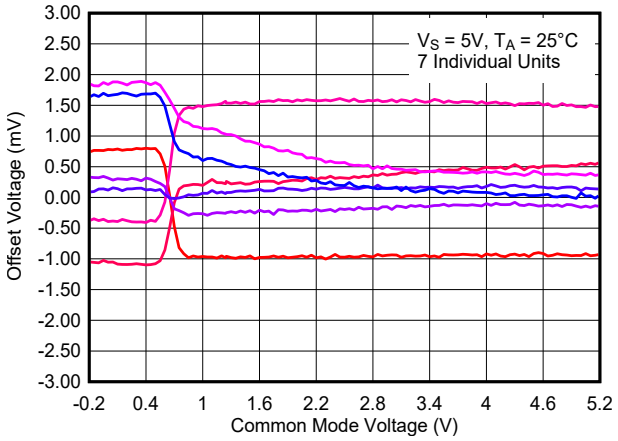

図 8-31. Offset Voltage vs. Common Mode Voltage, 5 V

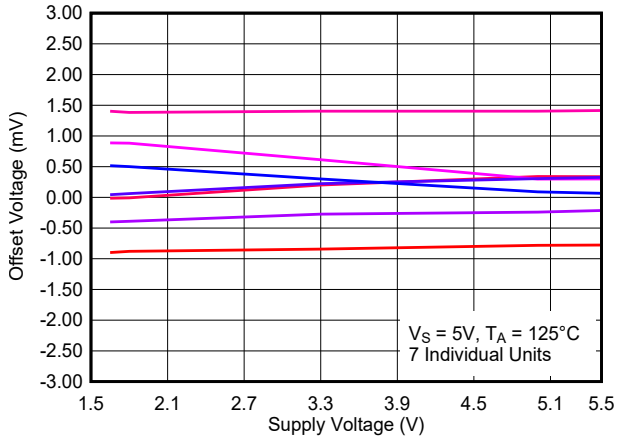

図 8-32. Offset Voltage vs. Supply Voltage, 125°C

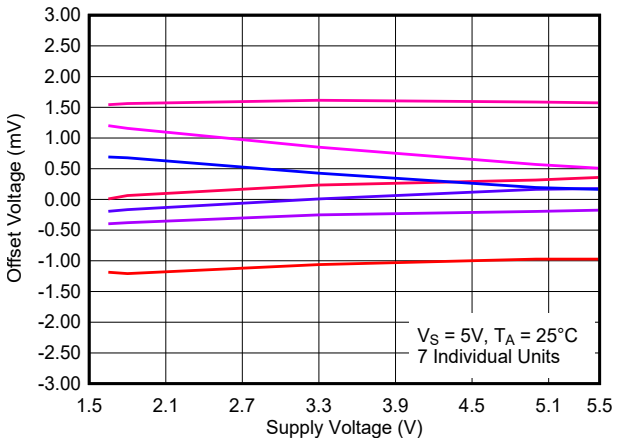

図 8-33. Offset Voltage vs. Supply Voltage, 25°C

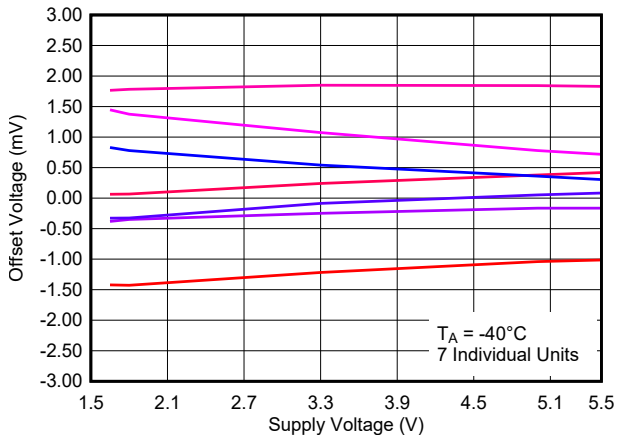

図 8-34. Offset Voltage vs. Supply Voltage, -40°C

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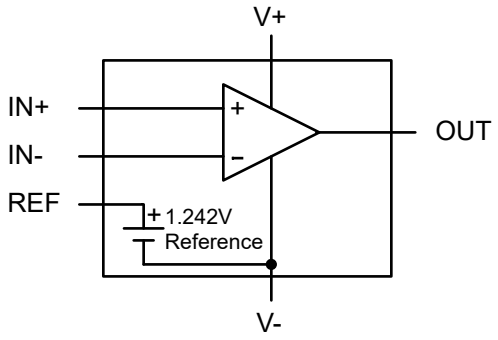
9 Detailed Description

9.1 Overview

The TLV301xB is a MicroPower comparator with an integrated reference that is well suited for compact, low-current, precision voltage detection applications. With a high-accuracy, internal reference of 1.242 V and 3.1 uA of quiescent current, the TLV301xB enables power conscious systems to monitor and respond quickly to fault conditions.

9.2 Functional Block Diagram



9.3 Feature Description

The TLV301x is comprised of a rail-to-rail input comparator with open-drain or push-pull output options and a voltage reference that is externally available.

9.4 Device Functional Modes

The TLV301x requires an operating voltage between 1.8 V and 5.5 V for the comparator output to reflect the voltage applied to the inputs. Similarly, the reference output (REF) will also be valid over the same operating voltage range. The "B" versions add hysteresis, power on reset, fail-safe inputs and a 1.65 V minimum supply voltage.

9.4.1 Open Drain Output (TLV3011 and TLV3011B)

The TLV3011 features an Open-Drain (sinking only) output that allows multiple devices to be driven by a single pull-up resistor to accomplish an OR function, making the TLV3011 useful for logic applications. The value of the pull-up resistor and supply voltage used will affect current consumption due to additional current drawn when the output is in a low state. This effect can be seen in the typical curve Quiescent Current vs Output Switching Frequency.

For the TLV3011, the pull-up voltage must be less than, or equal to, the V+ supply voltage ($V_{PULLUP} \leq V+$).

The TLV3011B may be pulled-up to any voltage up to 5.5V, regardless of the supply voltage.

9.4.2 Push-Pull Output (TLV3012 and TLV3012B)

The TLV3012 has a "Push-Pull" output capable of both sinking and sourcing current. The push-pull output stage is optimal for reduced power budget applications by eliminating the need for a pull-up resistor and features no shoot-through current. Do not tie push-pull outputs together.

9.4.3 Voltage Reference

The integrated 1.242-V voltage reference offers low 100-ppm/°C (maximum) drift provided on a seporate output pin that allows use of external dividers or to provide a reference voltage for other external circuitry. The reference is stable with up to a 10-nF capacitive load and can sink or source up to 500µA (typical) of output current.

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9.4.4 TLV3011B and TLV3012B Fail-Safe inputs

The TLV3011B and TLV3012B inputs are Fail-Safe up to 5.5V independent of V+ voltage. Fail-Safe is defined as maintaining the same high input impedance when V+ is unpowered or within the recommended operating ranges.

The Fail-Safe inputs can be any value between 0 V and 5.5 V, even while V+ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains its value even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state will be correct.

The following is a summary of the TLV3011B and TLV3012B device input voltage excursions and their outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output state is **indeterminate** (random). *Do not* operate in this region.

Because the inputs do not have upper ESD diode clamps to V+, input voltages must be externally clamped to below 5.5 V if the source could possibly exceed 5.5 V. A current limiting resistor in series with the input is also recommend in case of input transients.

9.4.5 TLV3011B and TLV3012B Power On Reset

The TLV3011B and TLV3012B have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry will be activated for up to 1.9ms after the minimum supply voltage threshold is crossed, or immediately when the supply voltage drops below minimum supply. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}). This delay is long enough to allow the reference output to stabilize with up to a 10nF capacitive load.

During the POR period (t_{on}), the outputs will be the following:

- The open drain output TLV3011B will be high (Hi-Z).
- The push-pull output TLV3012B will be low (sinking).

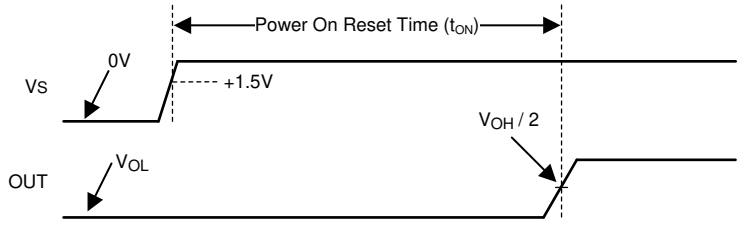

図 9-1. Power-On Reset Example Timing Diagram for Push-Pull Output

Note that it the nature of an open collector output that the output will rise with the pull-up voltage during the HI-Z POR period.

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10 Application and Implementation

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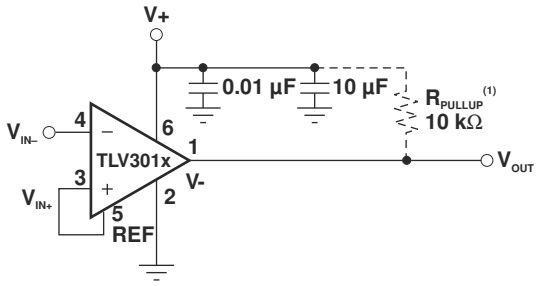
10.1 Application Information

The TLV301x and TLV301xB comparator family with on-chip 1.242-V series reference with the choice of either open-drain or push-pull output stages.

A typical supply current of 2.4 µA and small packaging combine with 1.65-V supply requirements to make the TLV301xB devices optimal for battery and portable designs.

図 10-1 shows the typical connections for the TLV3012 device.



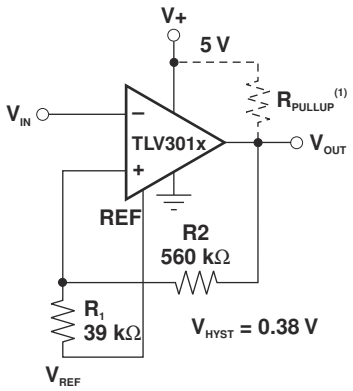
(1) Use R_{PULLUP} with the TLV3011 only.

図 10-1. Basic Connections

10.1.1 External Hysteresis

Comparator inputs have no noise immunity within the range of the specified offset voltage. For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV3012 device is ±0.5 mV. To prevent multiple switching within the comparator threshold of the TLV3012 device, external hysteresis may be added by connecting a small amount of feedback to the positive input. 図 10-2 shows a typical topology used to introduce hysteresis, described by 式 1.

$$V_{HYST} = \frac{V+ \times R1}{R1 + R2} \quad (1)$$



(1) Use R_{PULLUP} with the TLV3011 only.

図 10-2. Adding Hysteresis

The V_{HYST} voltage sets the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

10.1.2 TLV3011B and TLV3012B Hysteresis

The TLV3011B and TLV3012B have typically 6mV of built-in hysteresis. External hysteresis can still be added as explained in the previous section.

10.2 Typical Application

10.2.1 Under-Voltage Detection

Under-voltage detection is frequently required to alert the system that a battery voltage has dropped below the usable voltage level. Figure 23 shows a simple under-voltage detection circuit using the TLV3012 which is configured as a non-inverting comparator with the integrated 1.242 V reference is externally connected to the inverting input pin (IN-).

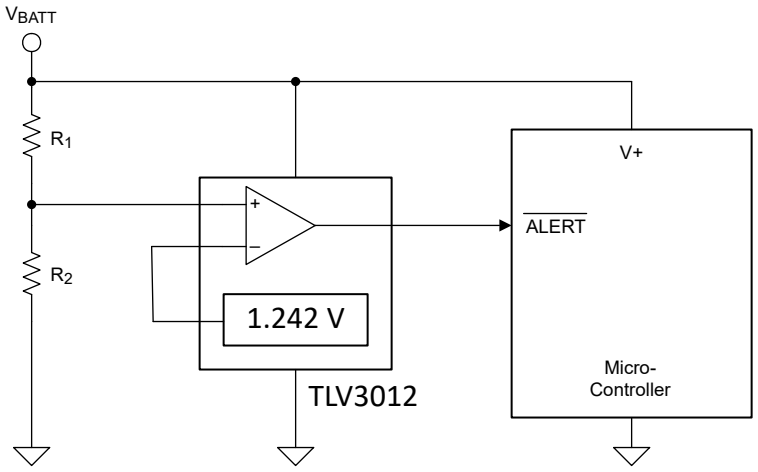


図 10-3. Under-Voltage Detection

10.2.1.1 Design Requirements

For this design, follow these design requirements:

- Operate from power supply that powers the microcontroller.
- Under-voltage alert is active low.
- Logic low output when V_{BAT} is less than 2.0V.

10.2.1.2 Detailed Design Procedure

Configure the circuit as shown in 図 10-3. Connect (V+) to V_{BAT} which also powers the microcontroller. Resistors R_1 and R_2 create the under-voltage alert level of 2.0 V. When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses V_{REF}, the 1.242 V reference threshold of the TLV3012. This causes the comparator output to transition from a logic high to a logic low. The push-pull output of the TLV3012 is selected since the comparator operating voltage is shared with the microcontroller which is receiving the under-voltage alert signal.

式 2 is derived from the analysis of 図 10-3.

$$V_{REF} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \tag{2}$$

where

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- R_1 and R_2 are the resistor values for the resistor divider connected to IN+
- V_{BAT} is the voltage source that is being monitored for an undervoltage condition.
- V_{REF} is the falling edge threshold where the comparator output changes state from high to low

Rearranging 式 2 and solving for R_1 yields 式 3.

$$R_1 = \frac{(V_{BAT} - V_{REF})}{V_{REF}} \times R_2 \tag{3}$$

For the specific undervoltage detection of 2.0 V using the TLV3012, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.242)}{1.242} \times 1M = 610\ k\Omega \tag{4}$$

where

- R_2 is set to 1 MΩ
- V_{BAT} is set to 2.0 V
- V_{REF} is set to1.242 V

Choose R_{TOTAL} (R_1 + R_2) such that the current through the divider is at least 100 times higher than the input bias current (I_{BIAS}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

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10.2.1.3 Application Curve

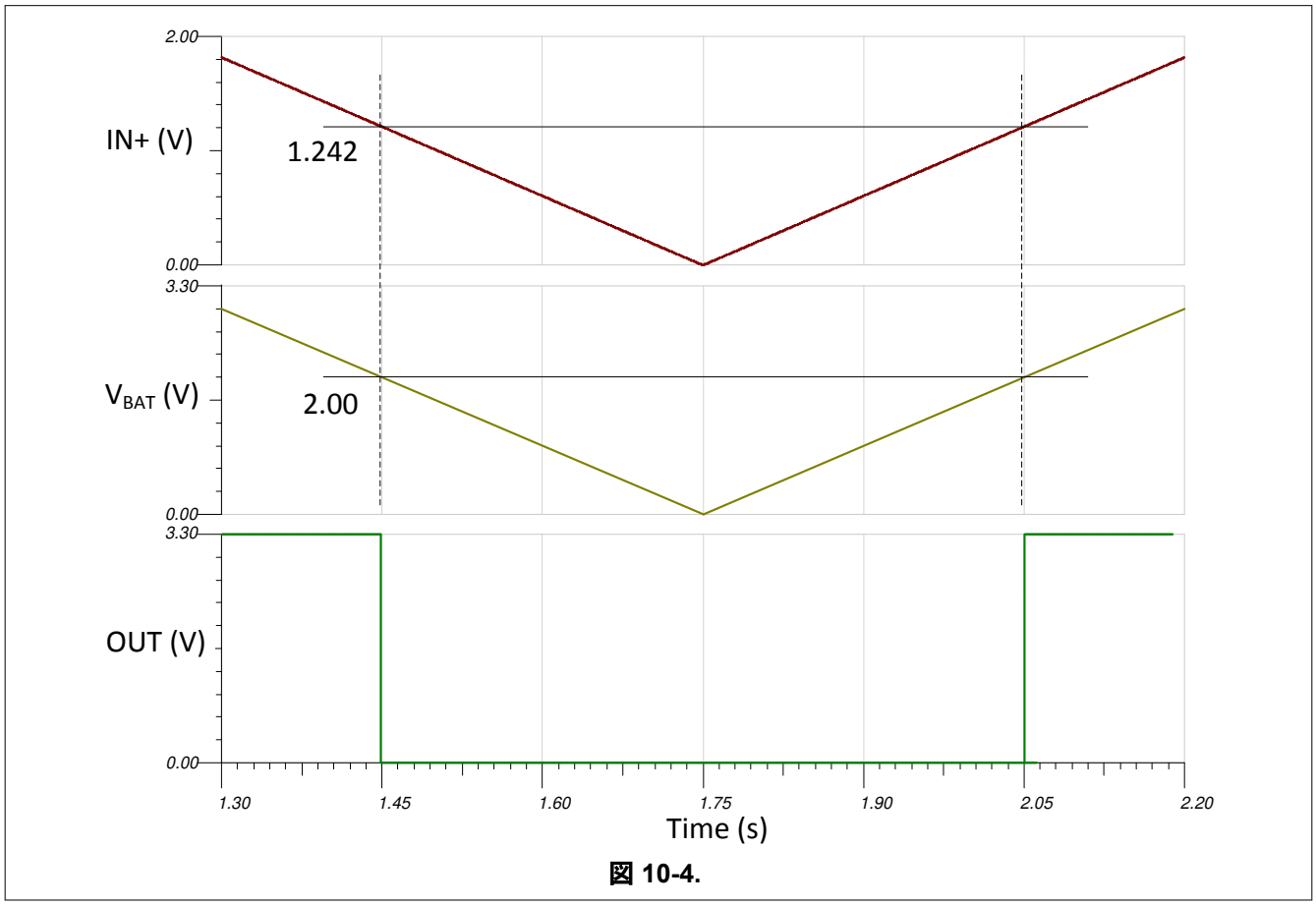

図 10-4.

10.3 System Examples

10.3.1 Power-On Reset

The reset circuit shown in 図 10-5 provides a time-delayed release of reset to the MSP430™ microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by the internal voltage reference. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state, releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit does not increase current consumption, because no current flows through the RC circuit after the supply has stabilized.

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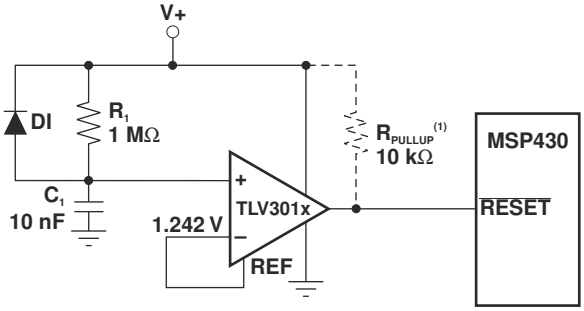

(1) Use R_{PULLUP} with the TLV3011 only.

図 10-5. TLV3012 Configured as Power-Up Reset Circuit for the MSP430™ Microcontroller

The reset delay needed depends on the power-up characteristics of the system power supply. R_1 and C_1 are selected to allow enough time for the power supply to stabilize. D_1 provides rapid reset if power is lost. In this example, the $R_1 \times C_1$ time constant is 10 ms.

10.3.2 Relaxation Oscillator

The TLV3012 device can be configured as a relaxation oscillator to provide a simple and inexpensive clock output (see 図 10-6). The capacitor is charged at a rate of T = 0.69RC and discharges at a rate of 0.69RC. Therefore, the period is T = 1.38RC. R_1 may be a different value than R_2.

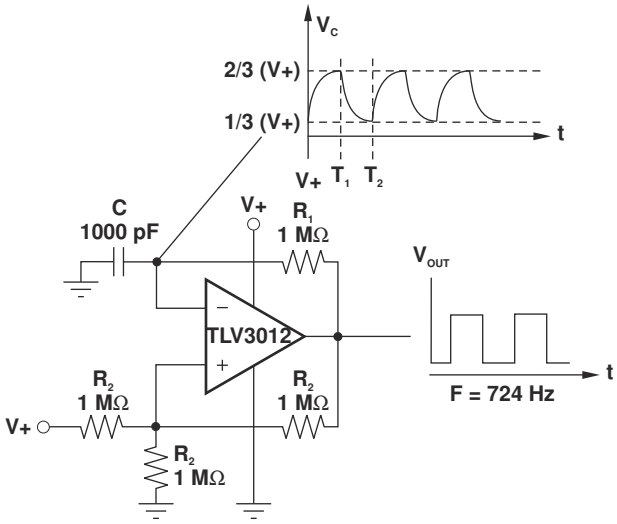

図 10-6. TLV3012 Configured as Relaxation Oscillator

10.4 Power Supply Recommendations

The TLV3012 has a recommended operating voltage range (V_S) of 1.8 V to 5.5 V. V_S is defined as (V+) – (V-). Therefore, the supply voltages used to create V_S can be single-ended or bipolar. For example, single-ended supply voltages of 5 V and 0 V and bipolar supply voltages of +2.5 V and –2.5 V create comparable operating voltages for V_S. However, when bipolar supply voltages are used, it is important to realize that the reference (REF) and logic low level of the comparator output is referenced to (V-). Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current in the EC Table.

10.5 Layout

10.5.1 Layout Guidelines

To minimize supply noise, power supplies should be capacitively decoupled by a 0.1-µF ceramic capacitor. Comparators are sensitive to input noise and precautions such as proper grounding (use of ground plane),

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supply bypassing, and guarding of high-impedance nodes minimize the effects of noise and help to ensure specified performance.

10.5.2 Layout Example

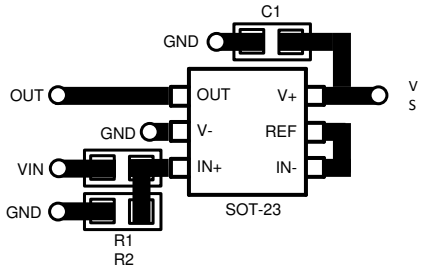

図 10-7. Layout Example

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11 Device and Documentation Support

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11.5 用語集

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12 Mechanical, Packaging, and Orderable Information

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3011AIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALR	Samples
TLV3011AIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALR	Samples
TLV3011AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALR	Samples
TLV3011AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	AJX	Samples
TLV3011AIDCKRG4	LIFEBUY	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AJX	
TLV3011AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	AJX	Samples
TLV3011AIDCKTG4	LIFEBUY	SC70	DCK	6	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	AJX	
TLV3011BIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31KF	Samples
TLV3011BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1O8	Samples
TLV3012AIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALS	Samples
TLV3012AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALS	Samples
TLV3012AIDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALS	Samples
TLV3012AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ALS	Samples
TLV3012AIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	ALT	Samples
TLV3012AIDCKRG4	LIFEBUY	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	ALT	
TLV3012AIDCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	ALT	Samples
TLV3012BIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31LF	Samples
TLV3012BIDCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1O9	Samples

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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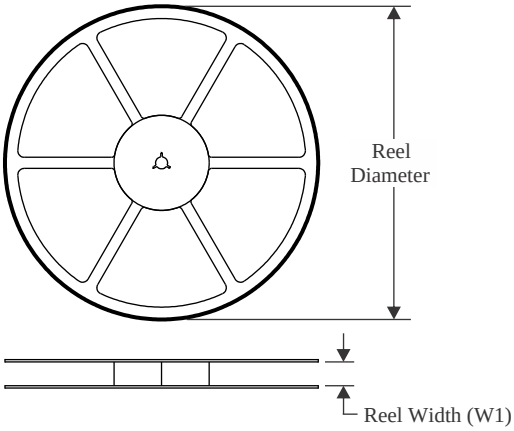
- Automotive : TLV3011-Q1, TLV3011B-Q1, TLV3012-Q1, TLV3012B-Q1
- Enhanced Product : TLV3011-EP, TLV3012-EP

NOTE: Qualified Version Definitions:

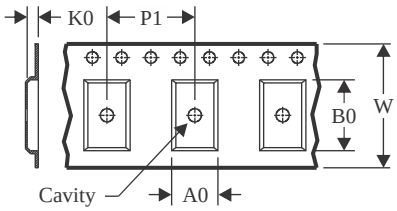
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

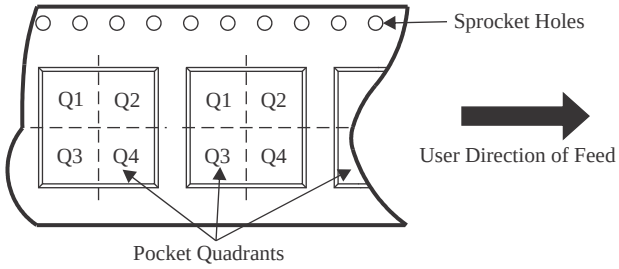


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

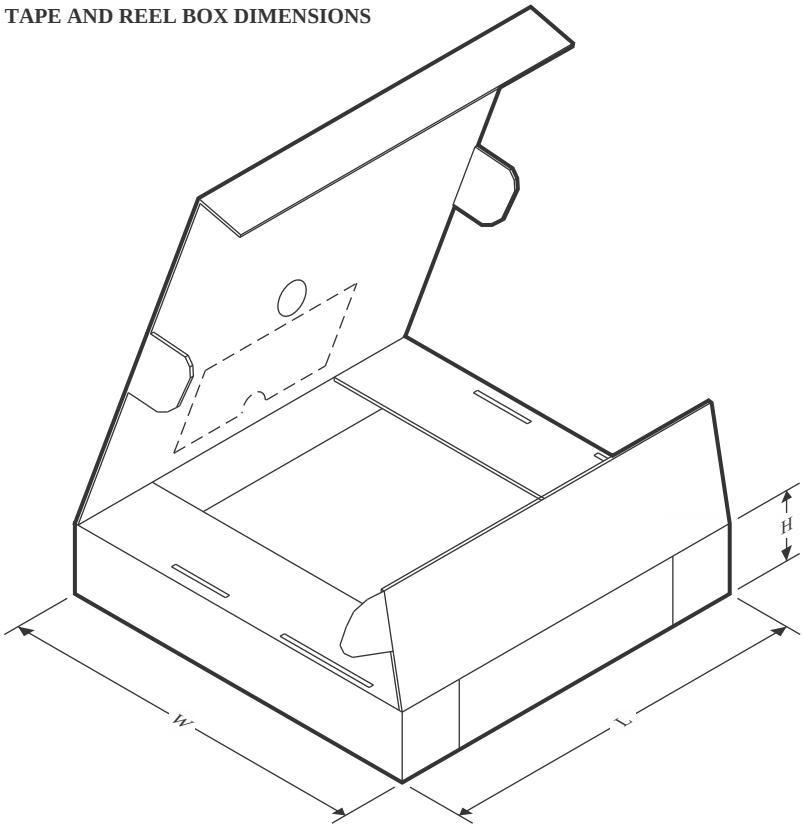
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3011AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3011AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3011AIDBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3011AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3011AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3011AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3011BIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3011BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3012AIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3012AIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3012AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3012AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3012AIDCKT	SC70	DCK	6	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3012BIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3012BIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

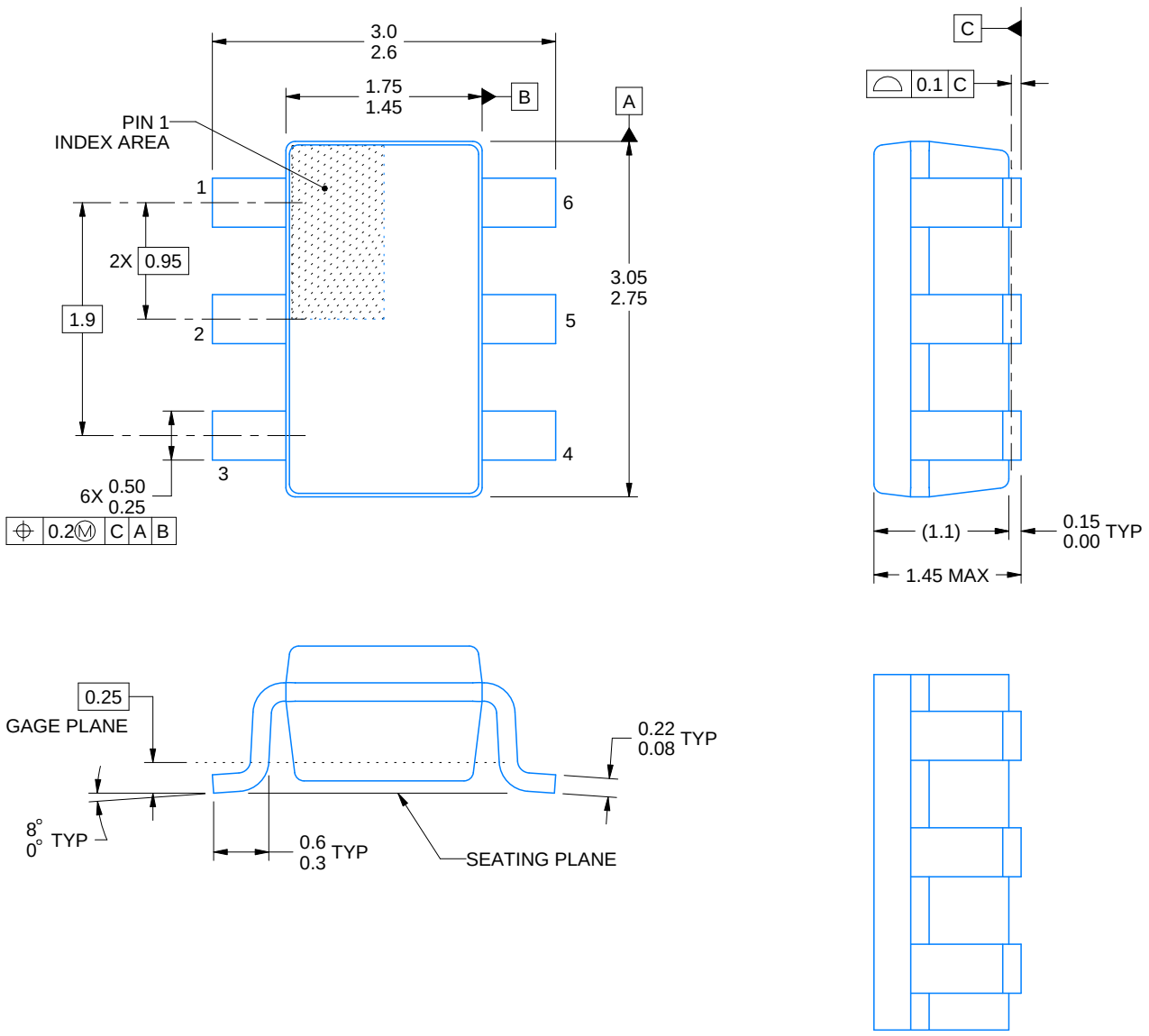
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3011AIDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV3011AIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3011AIDBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TLV3011AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3011AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3011AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
TLV3011BIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3011BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3012AIDBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV3012AIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3012AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3012AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV3012AIDCKT	SC70	DCK	6	250	180.0	180.0	18.0
TLV3012BIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV3012BIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

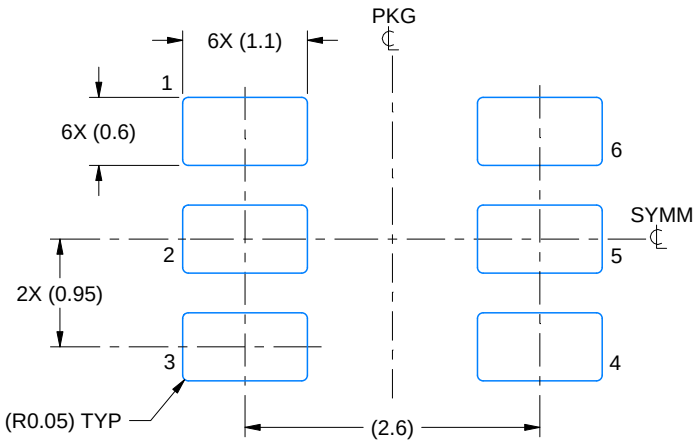


ALTERNATIVE PACKAGE SINGULATION VIEW

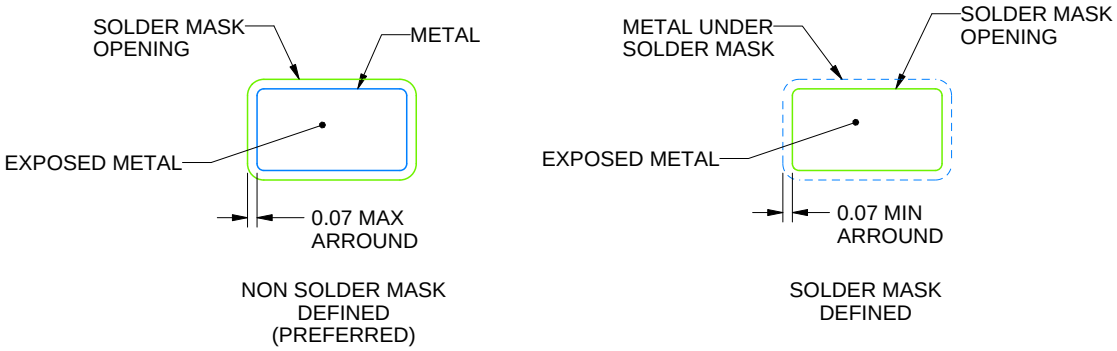
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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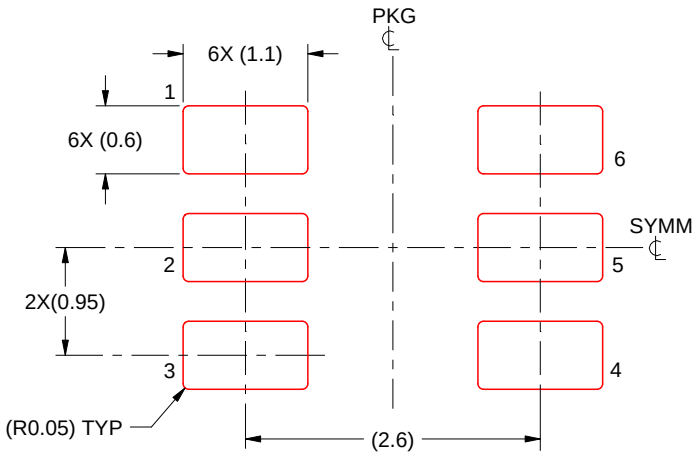
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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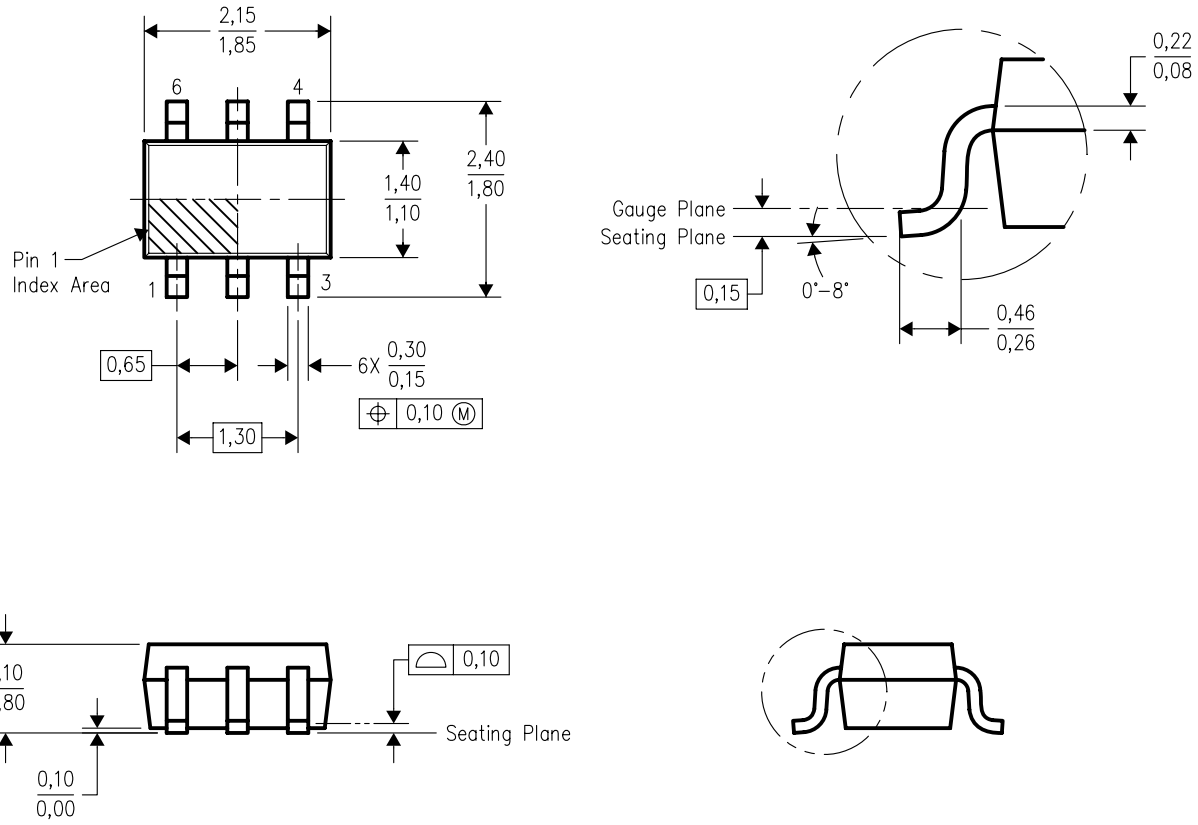
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

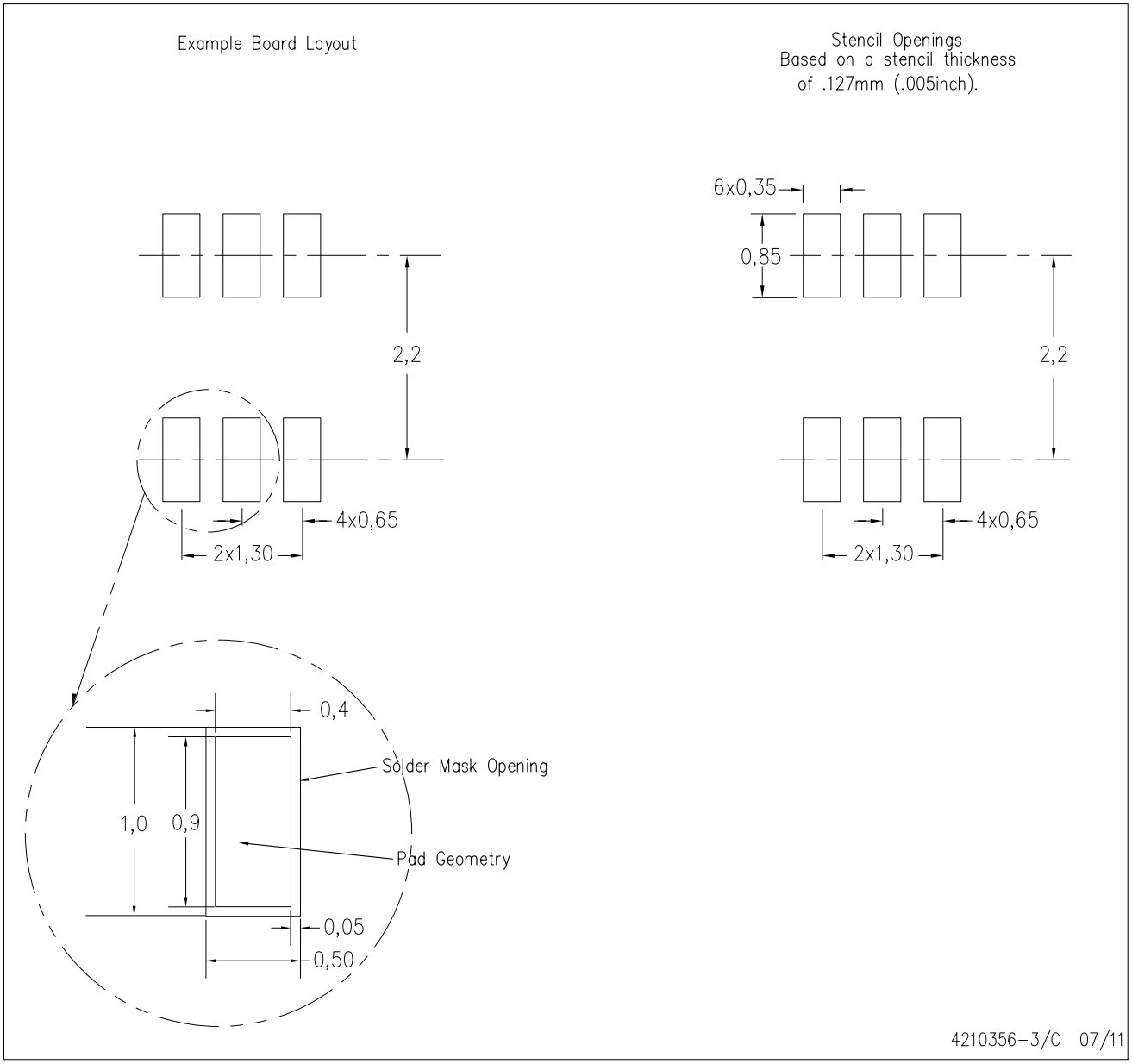
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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