TCA6424A 割り込み出力、リセット、構成レジスタ付き、低電圧 24 ビット I²C および SMBus I/O エクスパンダ

1 特長

- 1.65V～5.5V の動作電源電圧範囲
- 双方向の電圧レベル変換と、次の間の GPIO 拡張が可能：
  - 1.8V SCL/SDA と
    1.8V、2.5V、3.3V、5V の P ポート
  - 2.5V SCL/SDA と
    1.8V、2.5V、3.3V、5V の P ポート
  - 3.3V SCL/SDA と
    1.8V、2.5V、3.3V、5V の P ポート
  - 5V SCL/SDA と
    1.8V、2.5V、3.3V、5V の P ポート
- I^2C からパラレル・ポートへのエクスパンダ
- 低いスタンバイ消費電流：1μA
- シュミット・トリガ動作により、低速入力遷移が可能になり、SCL および SDA 入力でのスイッチング・ノイズ耐性が向上
  - V_{hys} = 0.18V (1.8V での標準値)
  - V_{hys} = 0.25V (2.5V での標準値)
  - V_{hys} = 0.33V (3.3V での標準値)
  - V_{hys} = 0.5V (5V での標準値)
- 5V 許容の I/O ポート
- アクティブ Low のリセット入力 ($\overline{RESET}$)
- オープンドレインのアクティブ Low 割り込み出力 ($\overline{INT}$)
- 400kHz の高速 I^2C バス
- 入力 / 出力構成レジスタ
- 極性反転レジスタ
- パワーオン・リセット内蔵
- 電源投入時はすべてのチャネルが入力に構成された状態
- 電源オン時のグリッチなし
- SCL/SDA 入力でのノイズ・フィルタ
- 大電流の最大駆動能力を持つラッチ付き出力により LED を直接駆動
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 200V、マシン・モデル (A115-A)
  - 1000V、デバイス帯電モデル (C101)

2 概要

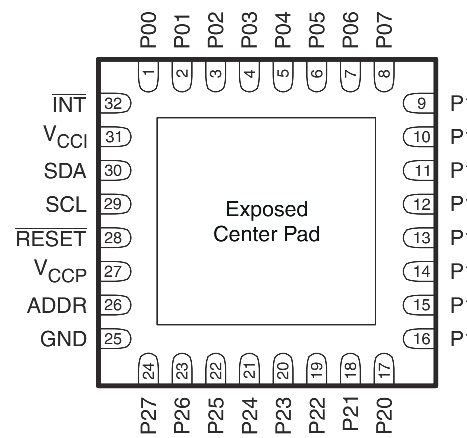
この 2 線式双方向バス (I^2C) 用 24 ビット I/O エクスパンダは、I^2C インターフェイス [シリアル・クロック (SCL) とシリアル・データ (SDA)] を介して、ほとんどのマイクロコントローラ・ファミリの汎用リモート I/O 拡張を実現できるように設計されています。

このデバイスの主な利点は、V_{CC} 範囲が広いことです。P ポート側と SDA/SCL 側で、1.65V～5.5V で動作可能です。このため、TCA6424A は SDA/SCL 側で、消費電力削減のため電源電圧レベルが引き下げられる次世代のマイクロプロセッサおよびマイクロコントローラと接続できます。マイクロプロセッサの電源供給は低下しますが、LED など PCB の部品には引き続き 5V の電源を供給します。

パッケージ情報

型番	パッケージ (1)	本体サイズ
TCA6424A	UQFN (32)	5.00mm × 5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



露出したセンター・パッドを使用する場合は、2 次側グランドとして接続するか、電気的に開放しておく必要があります。

RGJ パッケージ (底面図)

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3 Revision History

Changes from Revision C (April 2014) to Revision D (January 2023)	Page
• RSM パッケージへのすべての参照を削除	1
• I^2C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更	1
• Deleted Package thermal impedance from the *Absolute Maximum Ratings* table	6
• Added Storage temperature range to the *Absolute Maximum Ratings* table	6
• Changed Handling Ratings To: *ESD Ratings*	6
• Added the *Thermal Information* table	7
• Added the *Application and Implementation* NOTE	27
• Added the *Detailed Design Procedure* section	27
• Added paragraph: "Ramping up the device V_{CCP}" to *Power Supply Recommendations*	28

Changes from Revision B (September 2010) to Revision C (April 2014)	Page
• ハード・コーディングされた注文情報の表を削除。	1
• ドキュメントのフォーマットを更新	1

Changes from Revision A (August 2010) to Revision B (September 2010)	Page
• ドキュメントのステータスを「製品プレビュー」から「量産データ」に改訂。	1

Changes from Revision * (July 2010) to Revision A (August 2010)	Page
• Changed Recommended Supply Sequencing and Rates Table	28

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4 Description (continued)

The bidirectional voltage level translation in the TCA6424A is provided through V_{CCI}. V_{CCI} should be connected to the V_{CC} of the external SCL/SDA lines. This indicates the V_{CC} level of the I^2C bus to the TCA6424A. The voltage level on the P-port of the TCA6424A is determined by the V_{CCP}.

The TCA6424A consists of three 8-bit Configuration (input or output selection), Input, Output, and Polarity Inversion (active high) registers. At power on, the I/Os are configured as inputs. However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system controller.

The system controller can reset the TCA6424A in the event of a timeout or other improper operation by asserting a low in the $\overline{RESET}$ input. The power-on reset puts the registers in their default state and initializes the I^2C/SMBus state machine. The $\overline{RESET}$ pin causes the same reset/initialization to occur without depowering the part.

The TCA6424A open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed.

$\overline{INT}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA6424A can remain a simple target device.

The device P-port outputs have high-current sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I^2C address and allow up to two devices to share the same I^2C bus or SMBus.

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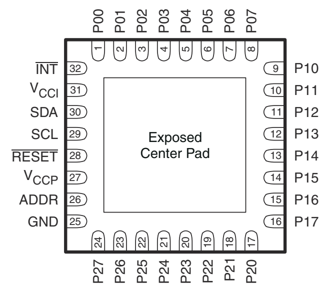
5 Pin Configuration and Functions



If used, the exposed center pad must be connected as a secondary ground or left electrically open.

図 5-1. RGJ Package (Bottom View)

表 5-1. Pin Functions

PIN		DESCRIPTION
PIN NO.	NAME	
1	P00	P-port input/output (push-pull design structure). At power on, P00 is configured as an input.
2	P01	P-port input/output (push-pull design structure). At power on, P01 is configured as an input.
3	P02	P-port input/output (push-pull design structure). At power on, P02 is configured as an input.
4	P03	P-port input/output (push-pull design structure). At power on, P03 is configured as an input.
5	P04	P-port input/output (push-pull design structure). At power on, P04 is configured as an input.
6	P05	P-port input/output (push-pull design structure). At power on, P05 is configured as an input.
7	P06	P-port input/output (push-pull design structure). At power on, P06 is configured as an input.
8	P07	P-port input/output (push-pull design structure). At power on, P07 is configured as an input.
9	P10	P-port input/output (push-pull design structure). At power on, P10 is configured as an input.
10	P11	P-port input/output (push-pull design structure). At power on, P11 is configured as an input.
11	P12	P-port input/output (push-pull design structure). At power on, P12 is configured as an input.
12	P13	P-port input/output (push-pull design structure). At power on, P13 is configured as an input.
13	P14	P-port input/output (push-pull design structure). At power on, P14 is configured as an input.
14	P15	P-port input/output (push-pull design structure). At power on, P15 is configured as an input.
15	P16	P-port input/output (push-pull design structure). At power on, P16 is configured as an input.
16	P17	P-port input/output (push-pull design structure). At power on, P17 is configured as an input.
17	P20	P-port input/output (push-pull design structure). At power on, P20 is configured as an input.
18	P21	P-port input/output (push-pull design structure). At power on, P21 is configured as an input.
19	P22	P-port input/output (push-pull design structure). At power on, P22 is configured as an input.
20	P23	P-port input/output (push-pull design structure). At power on, P23 is configured as an input.
21	P24	P-port input/output (push-pull design structure). At power on, P24 is configured as an input.
22	P25	P-port input/output (push-pull design structure). At power on, P25 is configured as an input.
23	P26	P-port input/output (push-pull design structure). At power on, P26 is configured as an input.
24	P27	P-port input/output (push-pull design structure). At power on, P27 is configured as an input.
25	GND	Ground
26	ADDR	Address input. Connect directly to V_{CCP} or ground.
27	V_{CCP}	Supply voltage of TCA6424A for P port
28	$\overline{RESET}$	Active-low reset input. Connect to V_{CCI} through a pullup resistor, if no active connection is used.
29	SCL	Serial clock bus. Connect to V_{CCI} through a pullup resistor.
30	SDA	Serial data bus. Connect to V_{CCI} through a pullup resistor.

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表 5-1. Pin Functions (continued)

PIN		DESCRIPTION
PIN NO.	NAME	
31	V_{CCI}	Supply voltage of I²C bus. Connect directly to the V_{CC} of the external I²C controller. Provides voltage-level translation.
32	$\overline{INT}$	Interrupt output. Connect to V_{CCI} through a pullup resistor.

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CCI}	Supply voltage range			–0.5	6.5	V
V_{CCP}	Supply voltage range			–0.5	6.5	V
V_I	Input voltage range[2]			–0.5	6.5	V
V_O	Output voltage range[2]			–0.5	6.5	V
I_{IK}	Input clamp current	ADDR, $\overline{RESET}$, SCL	$V_I < 0$		±20	mA
I_{OK}	Output clamp current	$\overline{INT}$	$V_O < 0$		±20	mA
I_{IOK}	Input/output clamp current	P port	$V_O < 0$ or $V_O > V_{CCP}$		±20	mA
		SDA	$V_O < 0$ or $V_O > V_{CCI}$		±20	
I_{OL}	Continuous output low current	P port	$V_O = 0$ to V_{CCP}		25	mA
		SDA, $\overline{INT}$	$V_O = 0$ to V_{CCI}		15	
I_{OH}	Continuous output high current	P port	$V_O = 0$ to V_{CCP}		25	mA
I_{CC}	Continuous current through GND				200	mA
	Continuous current through V_{CCP}				160	
	Continuous current through V_{CCI}				10	
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	01	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 2000 V may actually have higher performance.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CCI}	Supply voltage		1.65	5.5	V
V_{CCP}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CCI}$	VCCI	V
		$\overline{RESET}$	$0.7 \times V_{CCI}$	5.5	
		ADDR, P27–P00	$0.7 \times V_{CCP}$	5.5	
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{RESET}$	–0.5	$0.3 \times V_{CCI}$	V
		ADDR, P27–P00	–0.5	$0.3 \times V_{CCP}$	
I_{OH}	High-level output current	P27–P00		10	mA
I_{OL}	Low-level output current	P27–P00		25	mA
T_A	Operating free-air temperature		–40	85	°C

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6.4 Thermal Information

THERMAL METRIC[(1)]		TCA6424A RGJ (UQFN) 32 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	44.9	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	14.3	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	17.7	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.3	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	17.7	°C/W
$R_{θJC(bottom)}$	Junction-to-case (bottom) thermal resistance	9.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, V_{CCI} = 1.65 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCP}	MIN	TYP[(1)]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage	V_I = V_{CCP} or GND, I_O = 0	1.65 V to 5.5 V		1	1.4	V
V_{OH}	P-port high-level output voltage	I_{OH} = –8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		I_{OH} = –10 mA	1.65 V	1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4.0			
V_{OL}	P-port low-level output voltage	I_{OL} = 8mA	1.65 V			0.45	V
			2.3 V			0.25	
			3 V			0.25	
			4.5 V			0.23	
		I_{OL} = 10 mA	1.65 V			0.6	
			2.3 V			0.3	
			3 V			0.25	
			4.5 V			0.24	
I_{OL}	SDA	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			mA
	$\overline{INT}$	V_{OL} = 0.4 V	1.65 V to 5.5 V	3	15		
I_I	SCL, SDA, $\overline{RESET}$	V_I = V_{CCI} or GND	1.65 V to 5.5 V			±0.1	µA
	ADDR	V_I = V_{CCP} or GND				±0.1	
I_{IH}	P port	V_I = V_{CCP}	1.65 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND				1	µA

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6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range, V_{CCI} = 1.65 V to 5.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CCP}	MIN	TYP(1)	MAX	UNIT
I_{CC} (I_{CCP} + I_{CCI})	Operating mode	SDA, P port, ADDR, $\overline{\text{RESET}}$	V_I on SDA and $\overline{\text{RESET}}$= V_{CCI} or GND, V_I on P port and ADDR = V_{CCP}, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz	1.65 V to 5.5 V		8	30	µA
		SDA, P port, ADDR, $\overline{\text{RESET}}$	V_I on SDA and $\overline{\text{RESET}}$= V_{CCI} or GND, V_I on P port and ADDR = V_{CCP}, I_O = 0, I/O = inputs, f_{SCL} = 100 kHz	1.65 V to 5.5 V		1.7	10	
	Standby mode	SCL, SDA, P port, ADDR, $\overline{\text{RESET}}$	V_I on SCL, SDA and $\overline{\text{RESET}}$ = V_{CCI} or GND, V_I on P port and ADDR = V_{CCP}, I_O = 0, I/O = inputs, f_{SCL} = 0	1.65 V to 5.5 V		0.1	3	
ΔI_{CCI}	Additional current in Standby mode	SCL,SDA $\overline{\text{RESET}}$	One input at V_{CCI} – 0.6 V, Other inputs at V_{CCI} or GND	1.65 V to 5.5 V			25	µA
ΔI_{CCP}		P port, ADDR,	One input at V_{CCP} – 0.6 V, Other inputs at V_{CCP} or GND				60	
C_I	SCL		V_I = V_{CCI} or GND	1.65 V to 5.5 V		6	7	pF
C_{io}	SDA		V_{IO} = V_{CCI} or GND	1.65 V to 5.5 V		7	8	pF
	P port		V_{IO} = V_{CCP} or GND			7.5	8.5	

(1) Except for I_{CC}, all typical values are at nominal supply voltage (V_{CCP} = V_{CCI} =1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C. For I_{CC}, all typical values are at V_{CCP} = V_{CCI} = 3.3 V and T_A = 25°C.

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-1)

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency	0	100	0	400	kHz
t_{sch}	I²C clock high time	4		0.6		µs
t_{scl}	I²C clock low time	4.7		1.3		µs
t_{sp}	I²C spike time	0	50	0	50	ns
t_{sds}	I²C serial data setup time	250		100		ns
t_{sdh}	I²C serial data hold time	0		0		ns
t_{icr}	I²C input rise time		1000	20 + 0.1C_b (1)	300	ns
t_{icf}	I²C input fall time		300	20 + 0.1C_b (1)	300	ns
t_{ocf}	I²C output fall time; 10 pF to 400 pF bus		300	20 + 0.1C_b (1)	300	µs
t_{buf}	I²C bus free time between Stop and Start	4.7		1.3		µs
t_{sts}	I²C Start or repeater Start condition setup time	4.7		0.6		µs
t_{sth}	I²C Start or repeater Start condition hold time	4		0.6		µs
t_{sps}	I²C Stop condition setup time	4		0.6		µs
$t_{vd(data)}$	Valid data time; SCL low to SDA output valid		1		1	µs
$t_{vd(ack)}$	Valid data time of ACK condition; ACK signal from SCL low to SDA (out) low		1		1	µs

(1) C_b = total capacitance of one bus line in pF

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6.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-4)

		STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT
		MIN	MAX	MIN	MAX	
t_W	Reset pulse duration	4		4		ns
t_{REC}	Reset recovery time	0		0		ns
t_{RESET}	Time to reset[(1)]	600		600		ns

(1) Minimum time for SDA to become high or minimum time to wait before doing a START.

6.8 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see 図 7-1)

PARAMETER		FROM	TO	STANDARD MODE I^2C BUS		FAST MODE I^2C BUS		UNIT
				MIN	MAX	MIN	MAX	
t_{IV}	Interrupt valid time	P port	$\overline{INT}$		4		4	μs
t_{IR}	Interrupt reset delay time	SCL	$\overline{INT}$		4		4	μs
t_{PV}	Output data valid	SCL	P27–P00		400		400	ns
t_{PS}	Input data setup time	P port	SCL	0		0		ns
t_{PH}	Input data hold time	P port	SCL	300		300		ns

6.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

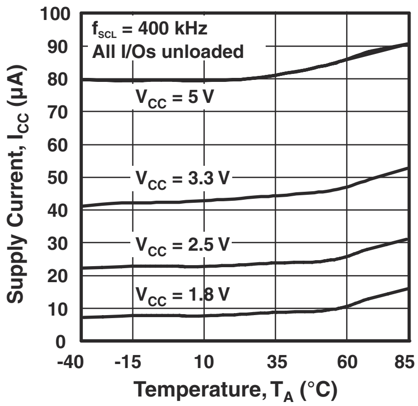

図 6-1. Supply Current vs Temperature

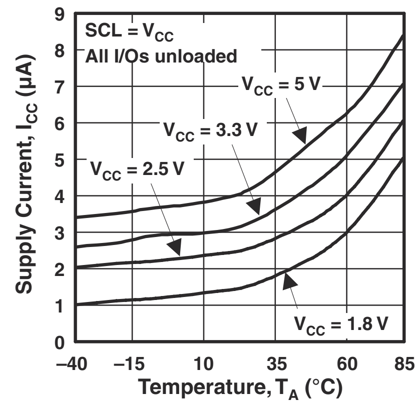

図 6-2. Standby Supply Current vs Temperature

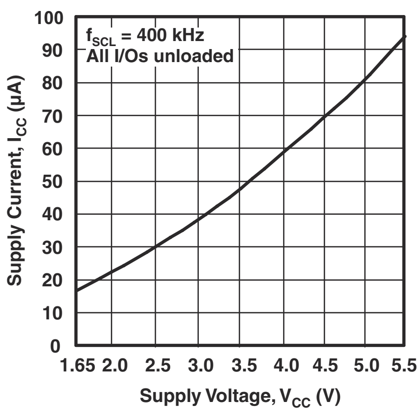

図 6-3. Supply Current vs Supply Voltage

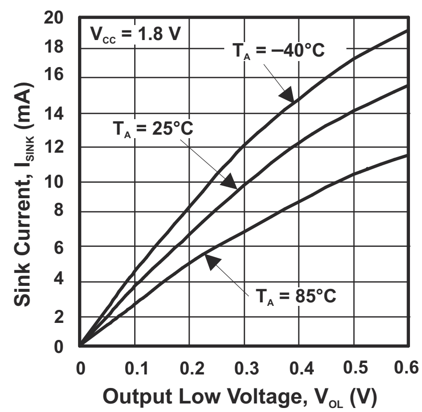

図 6-4. I/O Sink Current vs Output Low Voltage

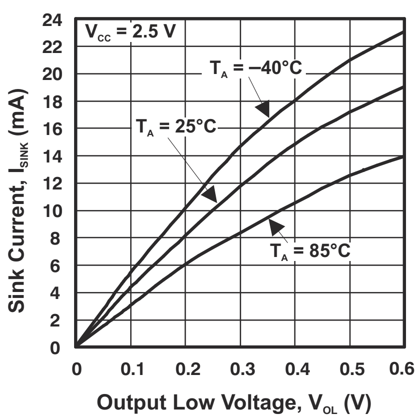

図 6-5. I/O Sink Current vs Output Low Voltage

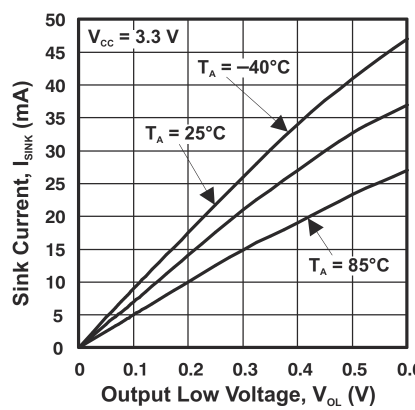

図 6-6. I/O Sink Current vs Output Low Voltage

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6.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

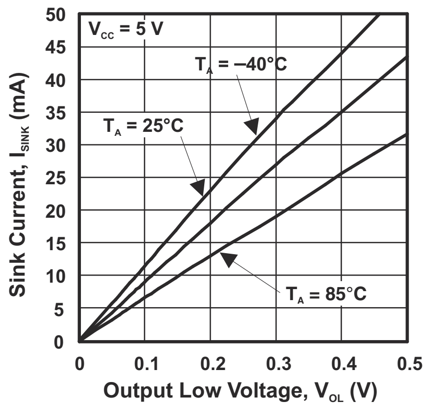

図 6-7. I/O Sink Current vs Output Low Voltage

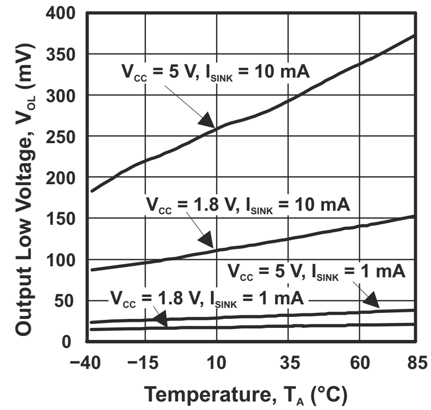

図 6-8. I/O Low Voltage vs Temperature

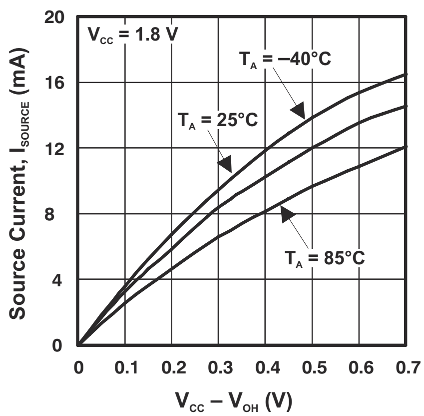

図 6-9. I/O Source Current vs Output High Voltage

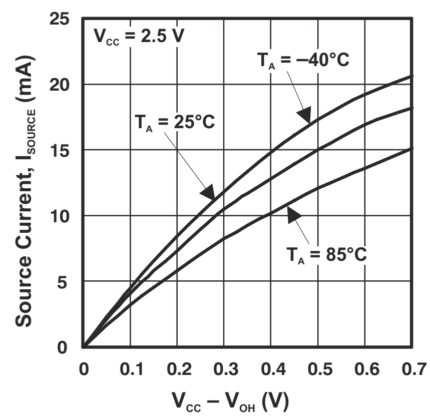

図 6-10. I/O Source Current vs Output High Voltage

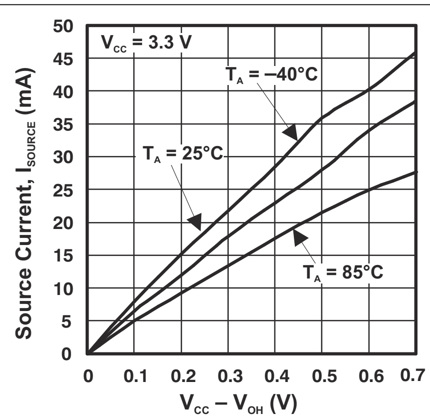

図 6-11. I/O Source Current vs Output High Voltage

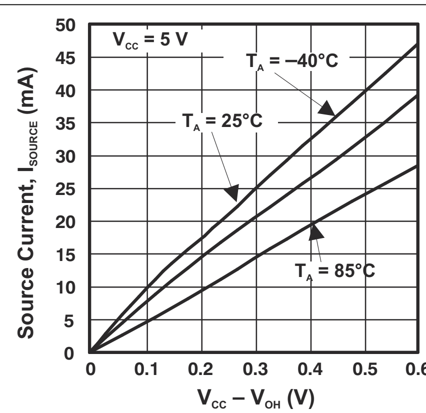

図 6-12. I/O Source Current vs Output High Voltage

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6.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

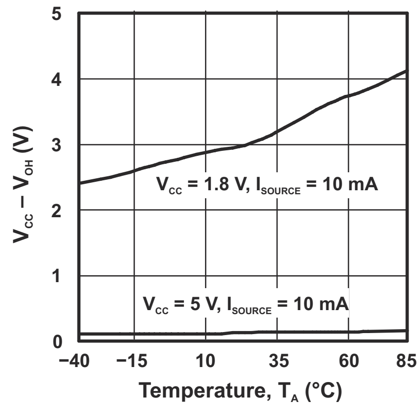

図 6-13. I/O High Voltage vs Temperature

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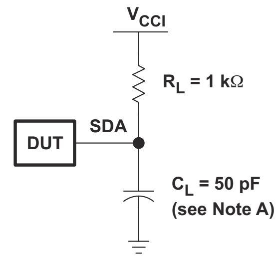
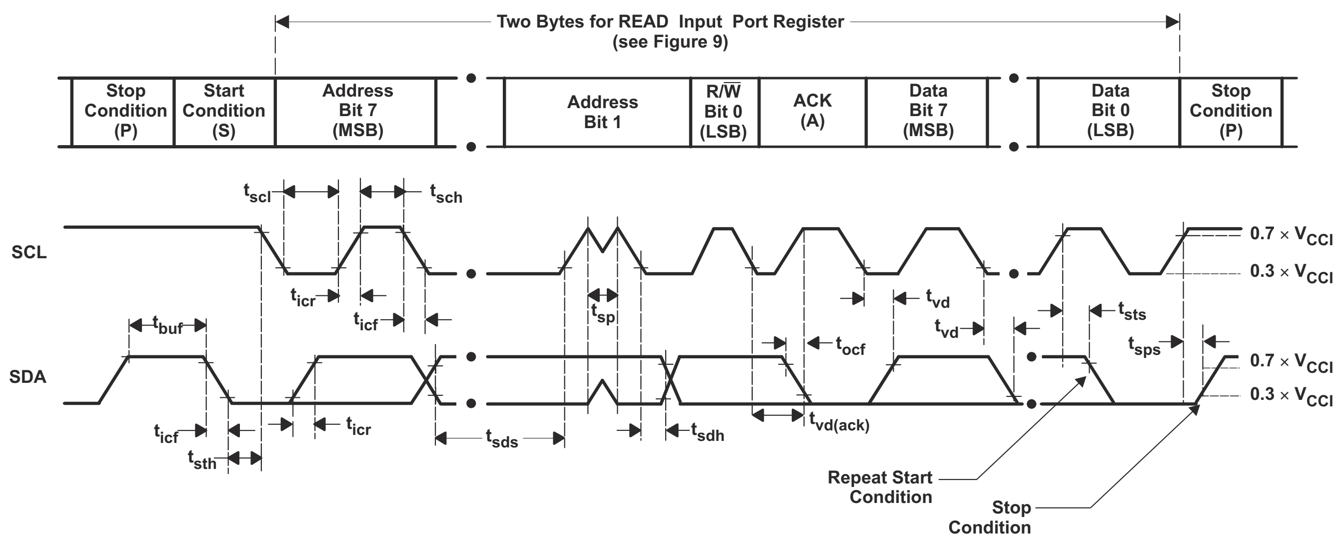
7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

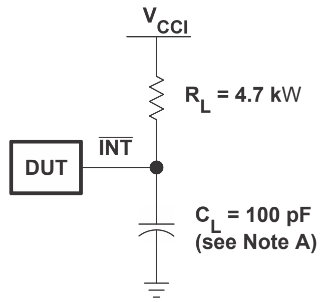
BYTE	DESCRIPTION
1	I2C address
2	Input register port data

A. C_L includes probe and jig capacitance. tocf is measured with C_L of 10 pF or 400 pF.

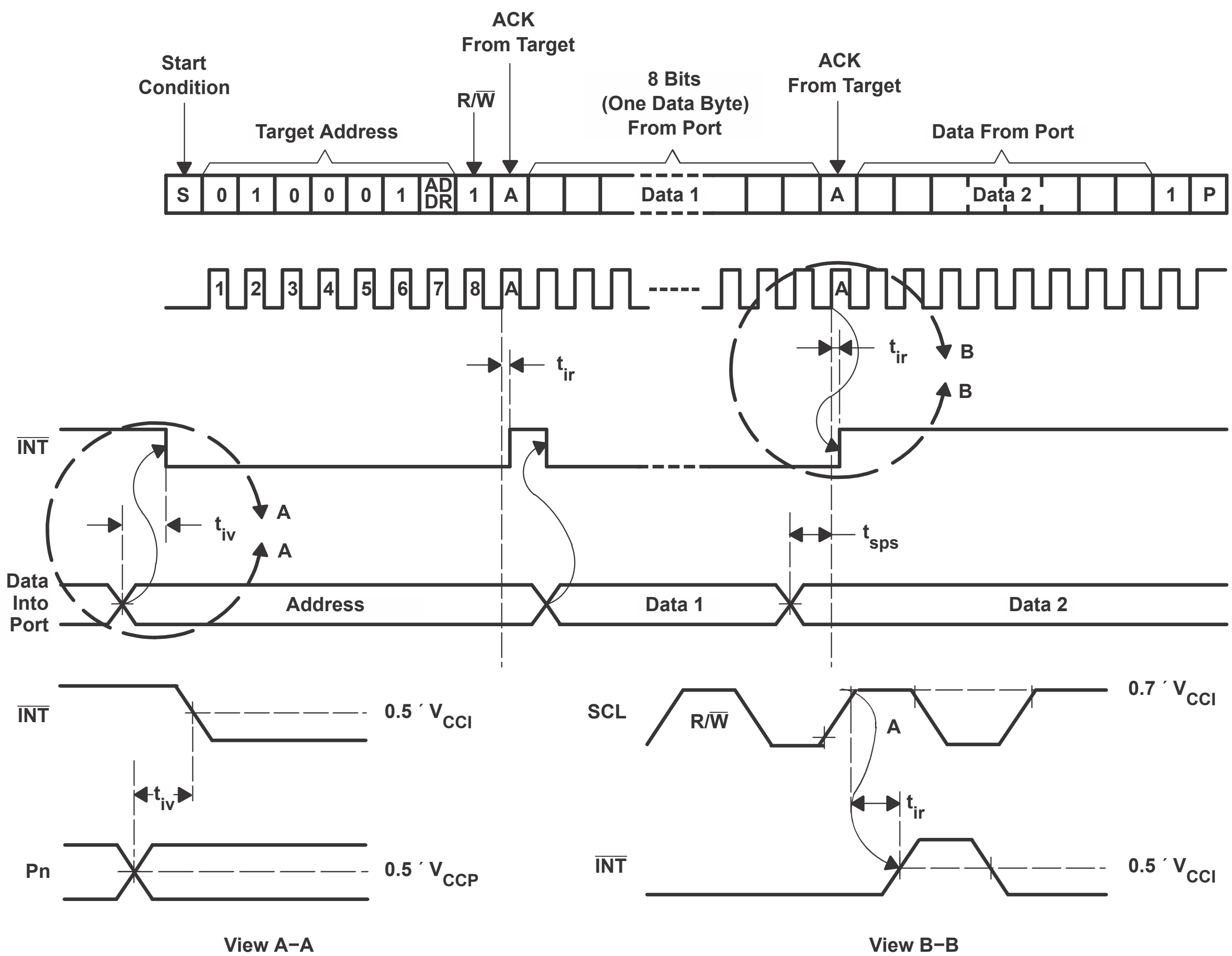
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. All parameters and waveforms are not applicable to all devices.

図 7-1. I²C Interface Load Circuit and Voltage Waveforms



INTERRUPT LOAD CONFIGURATION



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

図 7-2. Interrupt Load Circuit and Voltage Waveforms

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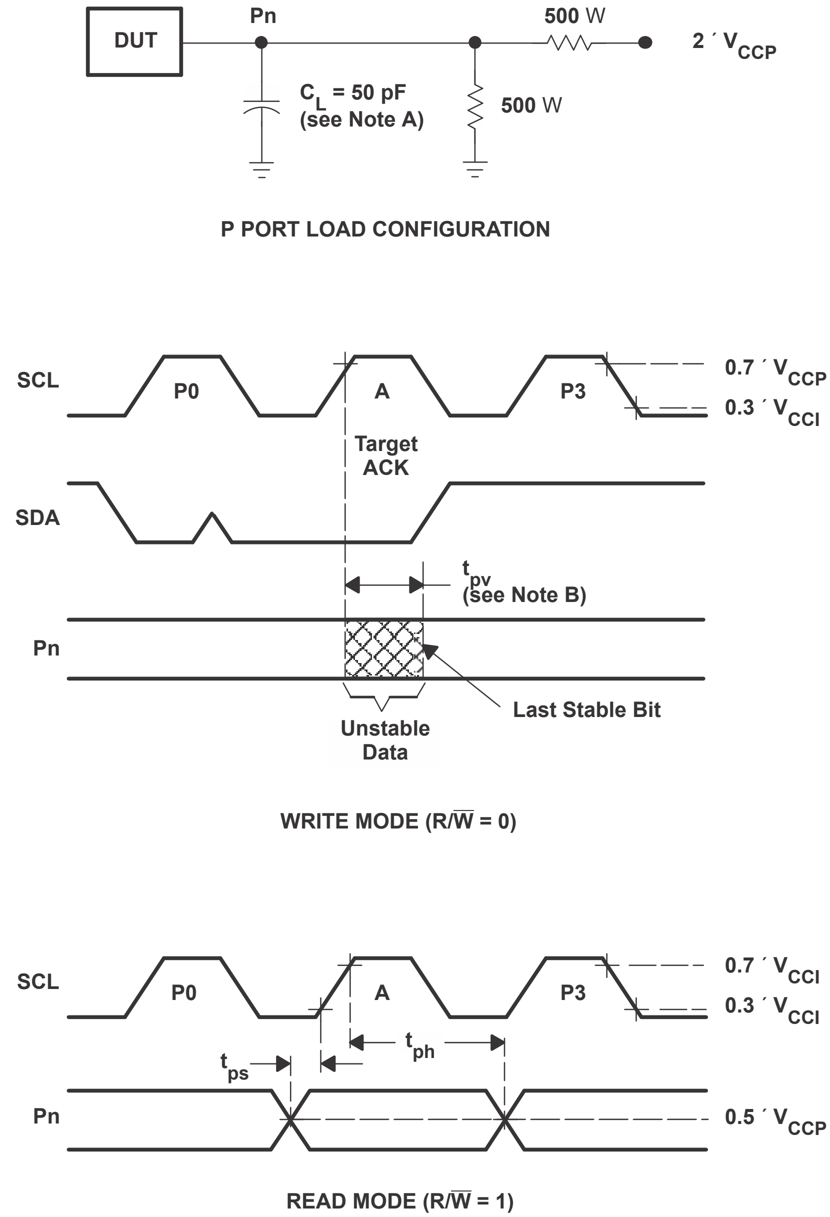
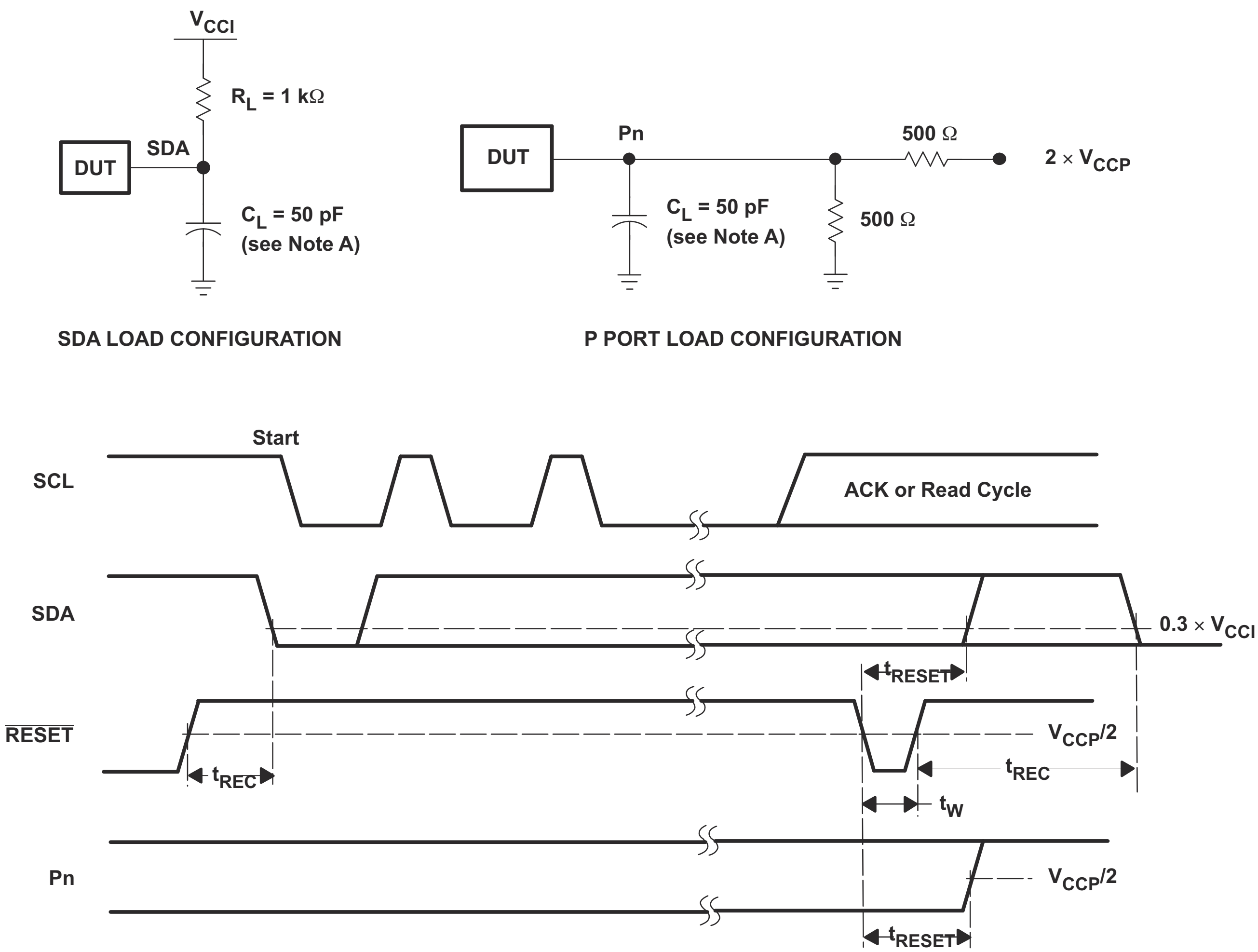


A. C_L includes probe and jig capacitance.
B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

図 7-3. P-Port Load Circuit and Timing Waveforms



A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

図 7-4. Reset Load Circuits and Voltage Waveforms

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8 Detailed Description

8.1 Overview

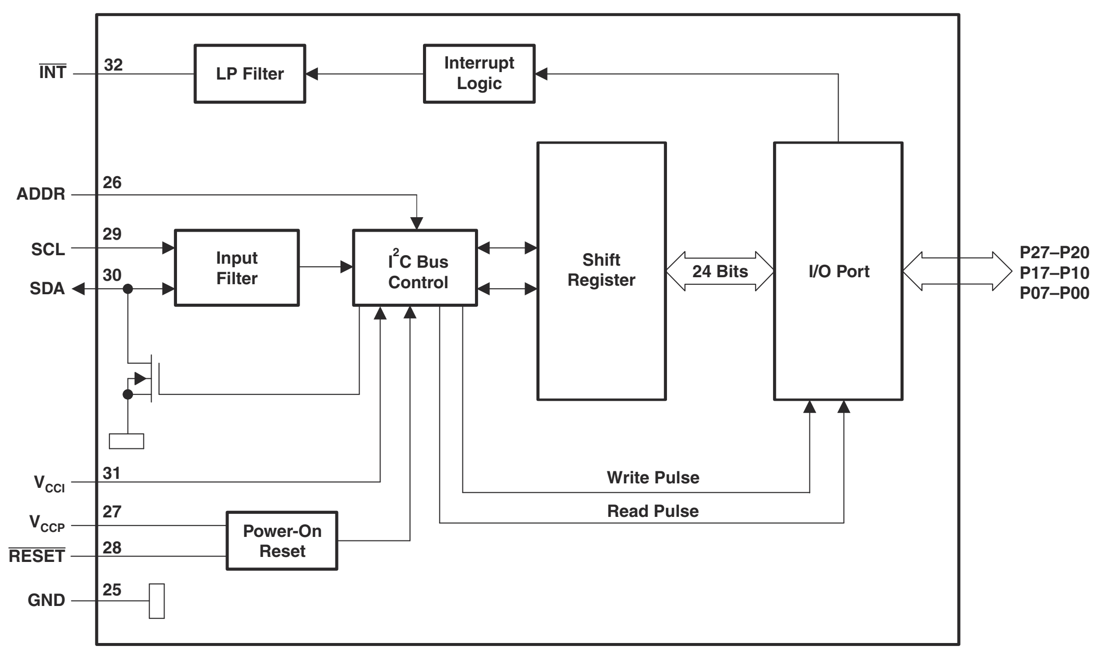
8.1.1 Voltage Translation

表 8-1 shows how to set up V_{CC} levels for the necessary voltage translation between the I^2C bus and the TCA6424A.

表 8-1. Voltage Translation

V_{CCI} (SDA AND SCL OF I^2C CONTROLLER) (V)	V_{CCP} (P PORT) (V)
1.8	1.8
1.8	2.5
1.8	3.3
1.8	5
2.5	1.8
2.5	2.5
2.5	3.3
2.5	5
3.3	1.8
3.3	2.5
3.3	3.3
3.3	5
5	1.8
5	2.5
5	3.3
5	5

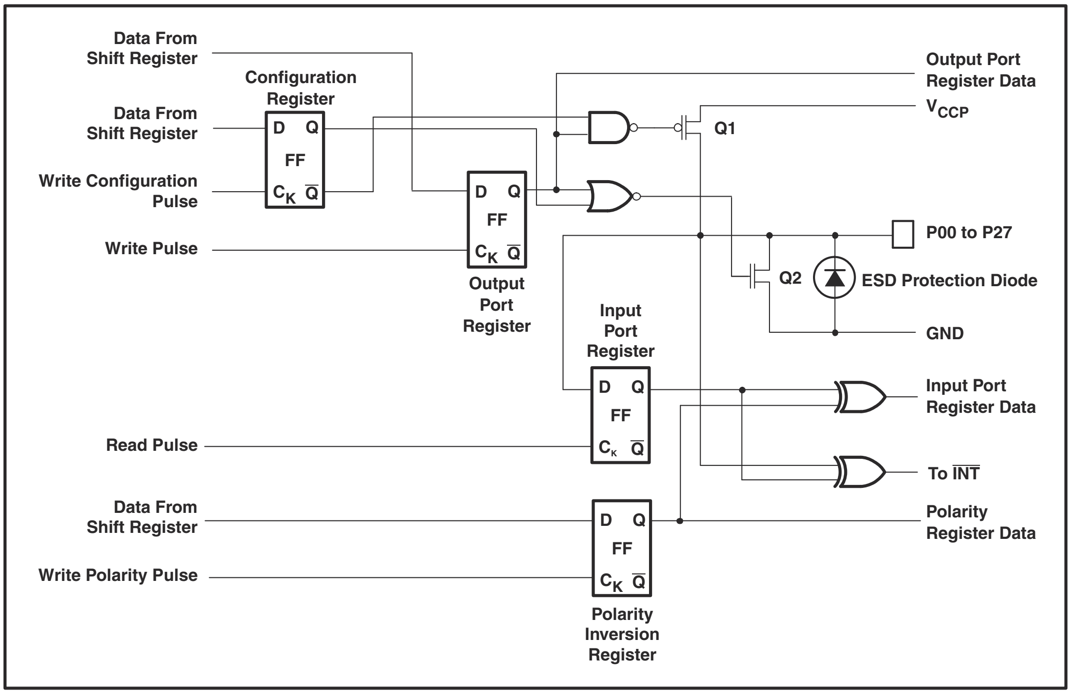
8.2 Functional Block Diagram



A. All I/Os are set to inputs at reset.

B. Pin numbers shown are for the RGJ package.

図 8-1. Positive Logic



A. On power up or reset, all registers return to default values.

図 8-2. Simplified Schematic of P00 to P27

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the output port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.3.2 I^{2}C Interface

The bidirectional I^{2}C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I^{2}C communication with this device is initiated by a controller sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high (see 図 8-3). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/$\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/ output during the high of the ACK-related clock pulse. The address (ADDR) input of the target device must not be changed between the Start and the Stop conditions.

On the I^{2}C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 図 8-4).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller (see 図 8-3).

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Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 図 8-5). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

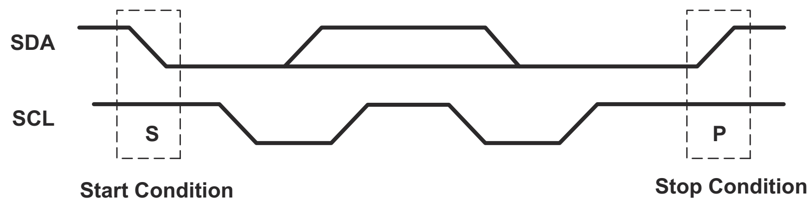

図 8-3. Definition of Start and Stop Conditions

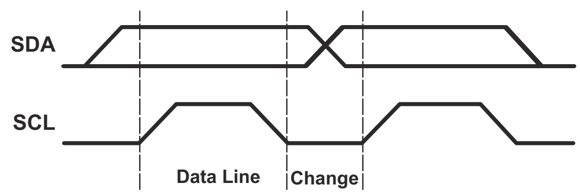

図 8-4. Bit Transfer

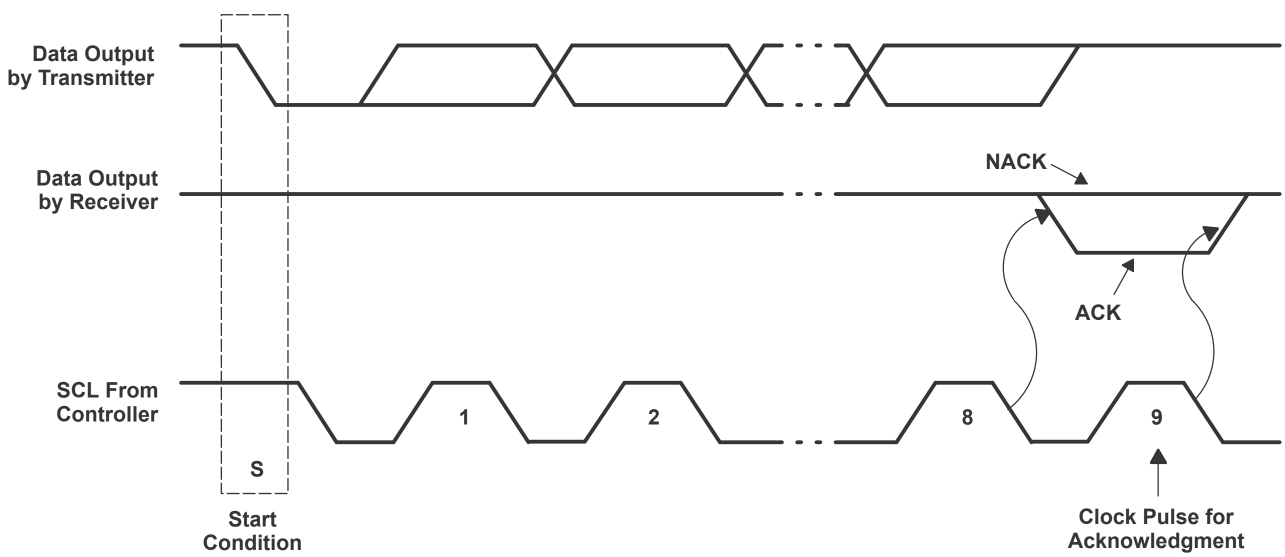

図 8-5. Acknowledgment on the I²C Bus

表 8-2. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C target address	L	H	L	L	L	H	ADDR	R/ $\overline{W}$

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表 8-2. Interface Definition (continued)

I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
	P17	P16	P15	P14	P13	P12	P11	P10
	P27	P26	P25	P24	P23	P22	P21	P20

8.4 Device Functional Modes

8.4.1 Device Address

The address of the TCA6424A is shown in 図 8-6.

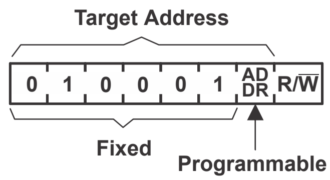

図 8-6. TCA6424A Address

表 8-3. Address Reference

ADDR	I²C BUS TARGET ADDRESS
L	34 (decimal), 22 (hexadecimal)
H	35 (decimal), 23 (hexadecimal)

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.5 Programming

8.5.1 Power-On Reset

When power (from 0 V) is applied to V_{CCP}, an internal power-on reset holds the TCA6424A in a reset condition until V_{CCP} has reached V_{POR}. At that time, the reset condition is released, and the TCA6424A registers and I^2C/SMBus state machine initializes to their default states. After that, V_{CCP} must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle.

8.5.2 Reset Input ($\overline{\text{RESET}}$)

The $\overline{\text{RESET}}$ input can be asserted to initialize the system while keeping the V_{CCP} at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TCA6424A registers and I^2C/SMBus state machine are changed to their default state once $\overline{\text{RESET}}$ is low (0). When $\overline{\text{RESET}}$ is high (1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pullup resistor to V_{CCI}, if no active connection is used.

8.5.3 Interrupt Output ($\overline{\text{INT}}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv}, the signal $\overline{\text{INT}}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or when data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{\text{INT}}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

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The $\overline{INT}$ output has an open-drain structure and requires pullup resistor to V_{CCP} or V_{CCI} depending on the application. If the $\overline{INT}$ signal is connected back to the processor that provides the SCL signal to the TCA6424A then the $\overline{INT}$ pin has to be connected to V_{CCI}. If not, the $\overline{INT}$ pin can be connected to V_{CCP}.

8.5.4 Bus Transactions

Data is exchanged between the controller and TCA6424A through write and read commands.

8.5.4.1 Writes

Data is transmitted to the TCA6424A by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission.

The twelve registers within the TCA6424A are grouped into four different sets. The four sets of registers are input ports, output ports, polarity inversion ports and configuration ports. After sending data to one register, the next data byte is sent to the next register in the group of 3 registers (see 図 8-7 and 図 8-8). For example, if the first byte is send to Output Port 2 (register 6), the next byte is stored in Output Port 0 (register 4).

There is no limitation on the number of data bytes sent in one write transmission. In this way, each 8-bit register may be updated independently of the other registers.

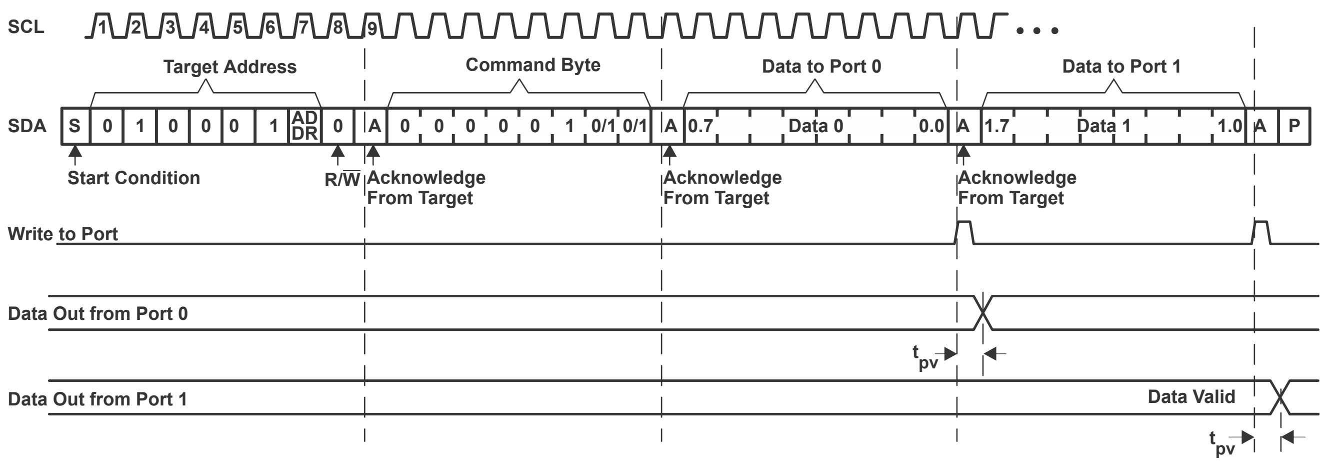


図 8-7. Write to Output Port Register

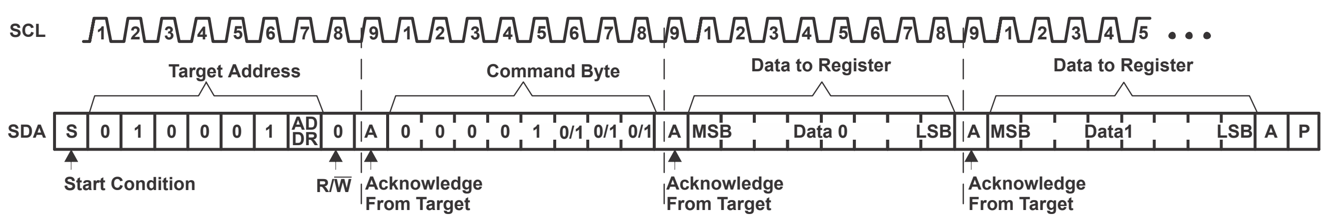


図 8-8. Write to Configuration or Polarity Inversion Registers

8.5.4.2 Reads

The bus controller first must send the TCA6424A address with the LSB set to a logic 0 (see 図 8-6 for device address). The command byte is sent after the address and determines which register is accessed.

After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the TCA6424A (see 図 8-9 and 図 8-10).

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus controller must not acknowledge the data.

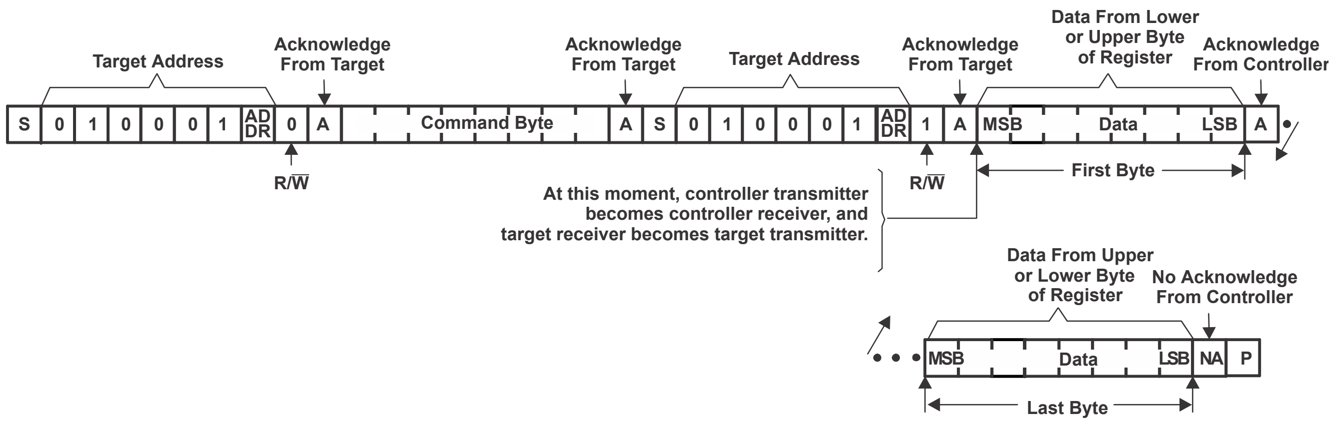
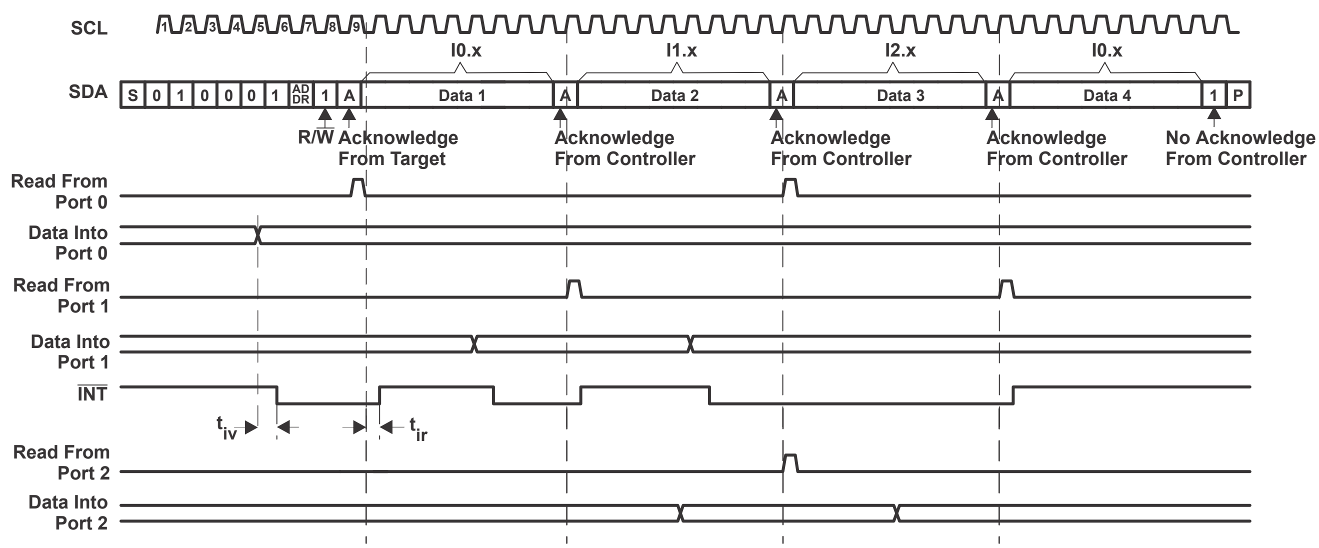


図 8-9. Read From Register



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and target address call between the initial target address call and actual data transfer from P port (see 図 8-9).

C. Auto-increment mode is enabled.

図 8-10. Read Input Port Register

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8.6 Register Maps

8.6.1 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte, which is stored in the control register in the TCA6424A. Four bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion, or configuration) that will be affected. The control register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

The control register includes an Auto-Increment (AI) bit which is the most significant bit (bit 7) of the command byte. At power-up, the control register defaults to 00 (hex), with the AI bit set to logic 1, and the lowest 7 bits set to logic 0.

If AI is 1, the 2 least significant bits are automatically incremented after a read or write. This allows the user to program and/or read the 3 register banks sequentially. If more than 3 bytes of data are written when AI is 1, previous data in the selected registers will be overwritten. Reserved registers are skipped and not accessed (refer to Table 5).

If AI is 0, the 2 least significant bits are not incremented after data is read or written. During a read operation, the same register bank is read each time. During a write operation, data is written to the same register bank each time.

Reserved command codes and command byte outside the range stated in the Command Byte table must not be accessed for proper device functionality.

AI	B6	B5	B4	B3	B2	B1	B0

図 8-11. Control Register Bits

表 8-4. Command Byte

CONTROL REGISTER BITS								AUTO-INCREMENT STATE	COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
AI	B6	B5	B4	B3	B2	B1	B0					
0	0	0	0	0	0	0	0	Disable	00	Input Port 0	Read byte	xxxx xxxx[1]
1	0	0	0	0	0	0	0	Enable	80			
0	0	0	0	0	0	0	1	Disable	01	Input Port 1	Read byte	xxxx xxxx[1]
1	0	0	0	0	0	0	1	Enable	81			
0	0	0	0	0	0	1	0	Disable	02	Input Port 2	Read byte	xxxx xxxx[1]
1	0	0	0	0	0	1	0	Enable	82			
0	0	0	0	0	0	1	1	Disable	03	Reserved	Reserved	Reserved
1	0	0	0	0	0	1	1	Enable	83			
0	0	0	0	0	1	0	0	Disable	04	Output Port 0	Read/write byte	1111 1111
1	0	0	0	0	1	0	0	Enable	84			
0	0	0	0	0	1	0	1	Disable	05	Output Port 1	Read/write byte	1111 1111
1	0	0	0	0	1	0	1	Enable	85			
0	0	0	0	0	1	1	0	Disable	06	Output Port 2	Read/write byte	1111 1111
1	0	0	0	0	1	1	0	Enable	86			
0	0	0	0	0	1	1	1	Disable	07	Reserved	Reserved	Reserved
1	0	0	0	0	1	1	1	Enable	87			
0	0	0	0	1	0	0	0	Disable	08	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	0	0	1	0	0	0	Enable	88			
0	0	0	0	1	0	0	1	Disable	09	Polarity Inversion Port 1	Read/write byte	0000 0000
1	0	0	0	1	0	0	1	Enable	89			
0	0	0	0	1	0	1	0	Disable	0A	Polarity Inversion Port 2	Read/write byte	0000 0000
1	0	0	0	1	0	1	0	Enable	8A			
0	0	0	0	1	0	1	1	Disable	0B	Reserved	Reserved	Reserved
1	0	0	0	1	0	1	1	Enable	8B			
0	0	0	0	1	1	0	0	Disable	0C	Configuration Port 0	Read/write byte	1111 1111
1	0	0	0	1	1	0	0	Enable	8C			
0	0	0	0	1	1	0	1	Disable	0D	Configuration Port 1	Read/write byte	1111 1111
1	0	0	0	1	1	0	1	Enable	8D			
0	0	0	0	1	1	1	0	Disable	0E	Configuration Port 2	Read/write byte	1111 1111
1	0	0	0	1	1	1	0	Enable	8E			
0	0	0	0	1	1	1	1	Disable	0F	Reserved	Reserved	Reserved
1	0	0	0	1	1	1	1	Enable	8F			

(1) Undefined

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8.6.2 Register Descriptions

The Input Port registers (registers 0, 1 and 2) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. They act only on read operation. Writes to these registers have no effect. The default value (X) is determined by the externally applied logic level. Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register will be accessed next.

表 8-5. Registers 0, 1 and 2 (Input Port Registers)

BIT	I-07	I-06	I-05	I-04	I-03	I-02	I-01	I-00
DEFAULT	X	X	X	X	X	X	X	X
BIT	I-17	I-16	I-15	I-14	I-13	I-12	I-11	I-10
DEFAULT	X	X	X	X	X	X	X	X
BIT	I-27	I-26	I-25	I-24	I-23	I-22	I-21	I-20
DEFAULT	X	X	X	X	X	X	X	X

The Output Port registers (registers 4, 5 and 6) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

表 8-6. Registers 4, 5 and 6 (Output Port Registers)

BIT	O-07	O-06	O-05	O-04	O-03	O-02	O-01	O-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	O-17	O-16	O-15	O-14	O-13	O-12	O-11	O-10
DEFAULT	1	1	1	1	1	1	1	1
BIT	O-27	O-26	O-25	O-24	O-23	O-22	O-21	O-20
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 8, 9 and 10) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in these registers is cleared (written with a 0), the corresponding port pin's original polarity is retained.

表 8-7. Registers 8, 9 and 10 (Polarity Inversion Registers)

BIT	P-07	P-06	P-05	P-04	P-03	P-02	P-01	P-00
DEFAULT	0	0	0	0	0	0	0	0
BIT	P-17	P-16	P-15	P-14	P-13	P-12	P-11	P-10
DEFAULT	0	0	0	0	0	0	0	0
BIT	P-27	P-26	P-25	P-24	P-23	P-22	P-21	P-20
DEFAULT	0	0	0	0	0	0	0	0

The Configuration registers (registers 12, 13 and 14) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output.

表 8-8. Registers 12, 13 and 14 (Configuration Registers)

BIT	C-07	C-06	C-05	C-04	C-03	C-02	C-01	C-00
DEFAULT	1	1	1	1	1	1	1	1
BIT	C-17	C-16	C-15	C-14	C-13	C-12	C-11	C-10
DEFAULT	1	1	1	1	1	1	1	1
BIT	C-27	C-26	C-25	C-24	C-23	C-22	C-21	C-20

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表 8-8. Registers 12, 13 and 14 (Configuration Registers) (continued)

DEFAULT	1	1	1	1	1	1	1	1

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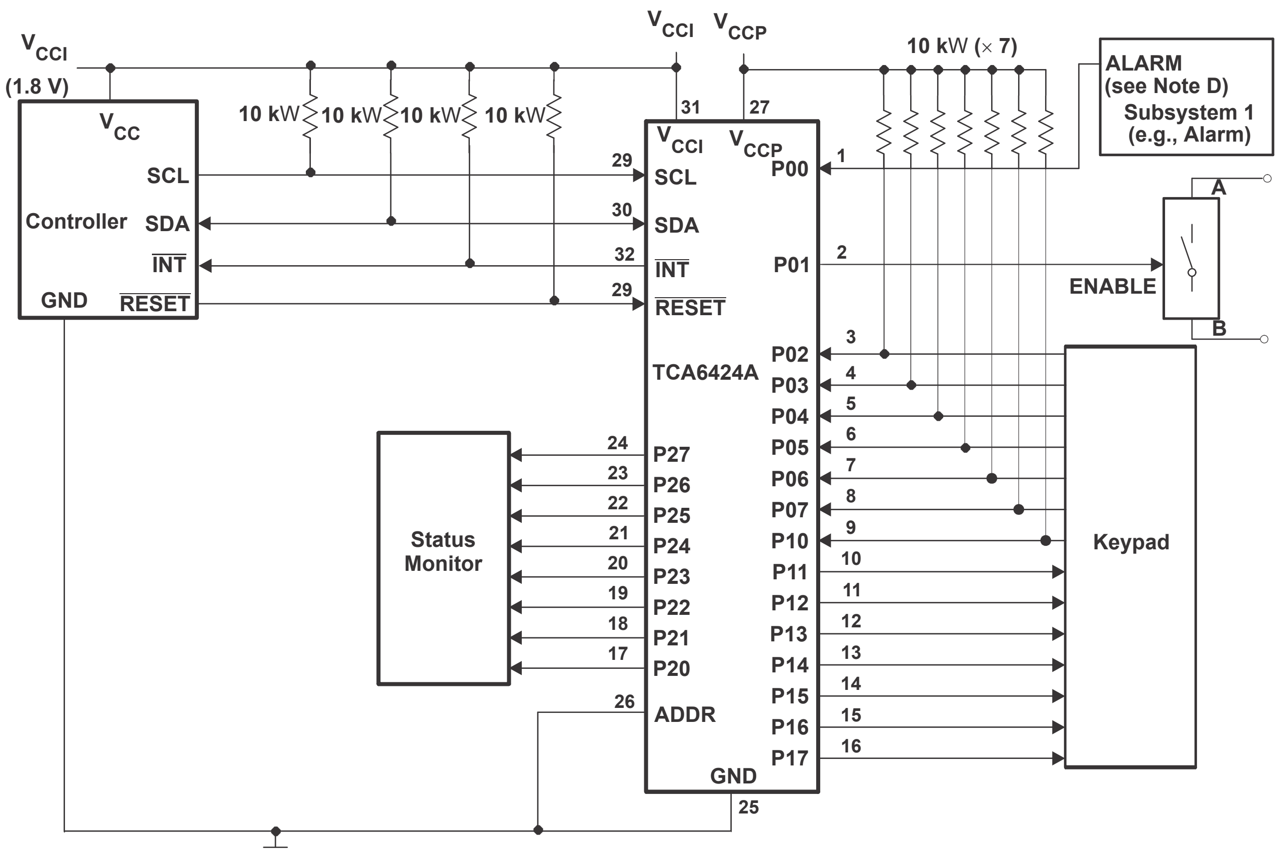
9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

図 9-1 shows an application in which the TCA6424A can be used.



A. Device address configured as 0100000 for this example.
B. P00 and P02–P10 are configured as inputs.
C. P01, P11–P17, and P20–P27 are configured as outputs.
D. Resistors are required for inputs (on P port) that may float. If a driver to an input will not let the input float, a resistor is not needed. Outputs (in the P port) do not need pullup resistors.

図 9-1. Typical Application

9.1.1 Detailed Design Procedure

9.1.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in 図 9-1. The LED acts as a diode so, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. Designs that must minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{CC} when the LED is off.

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図 9-2 shows a high-value resistor in parallel with the LED. 図 9-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevent additional supply current consumption when the LED is off.

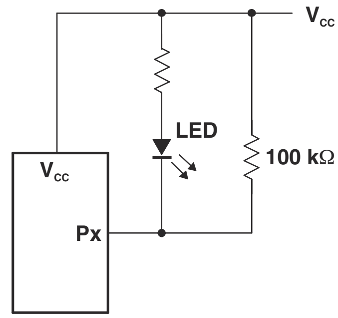

図 9-2. High-Value Resistor in Parallel With the LED

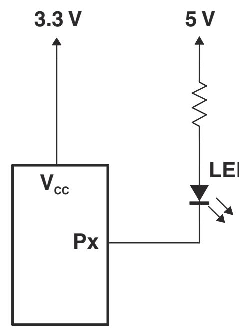

図 9-3. Device Supplied by a Low Voltage

9.2 Power Supply Recommendation

In the event of a glitch or data corruption, TCA6424A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

Ramping up the device V_{CCP} before V_{CCI} is recommended to prevent SDA from potentially being stuck LOW.

The two types of power-on reset are shown in 図 9-4 and 図 9-5.

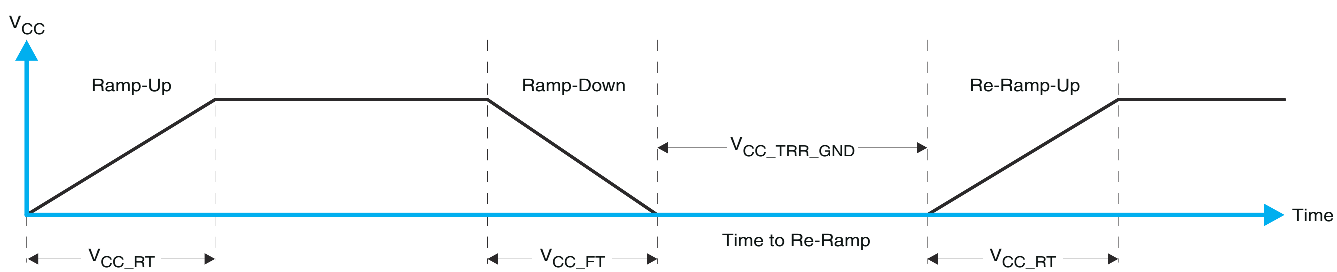

図 9-4. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

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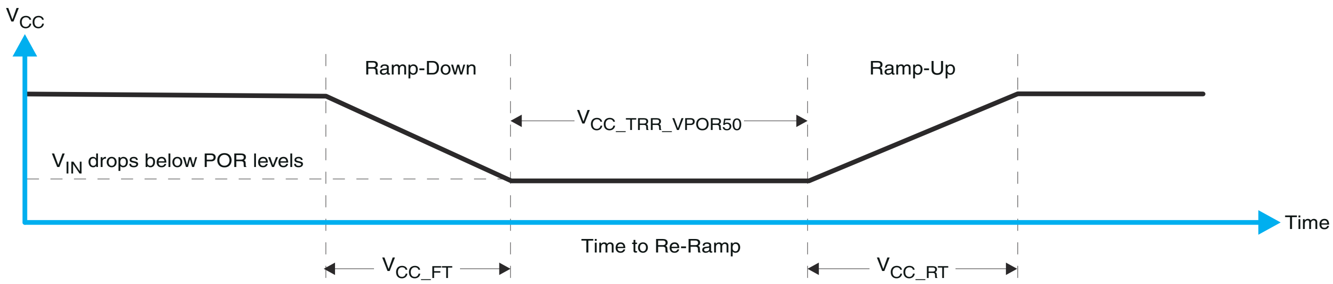

図 9-5. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

表 9-1 specifies the performance of the power-on reset feature for TCA6424A for both types of power-on reset.

表 9-1. Recommended Supply Sequencing and Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
t_{VCC_FT}	Fall rate	See 図 9-4	1		100	ms
t_{VCC_RT}	Rise rate	See 図 9-4	0.01		100	ms
$t_{VCC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 図 9-4	40			μs
$t_{VCC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 図 9-5	40			μs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs	See 図 9-6			1.2	V
t_{VCC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 図 9-6			10	μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. 図 9-6 and 表 9-1 provide more information on how to measure these specifications.

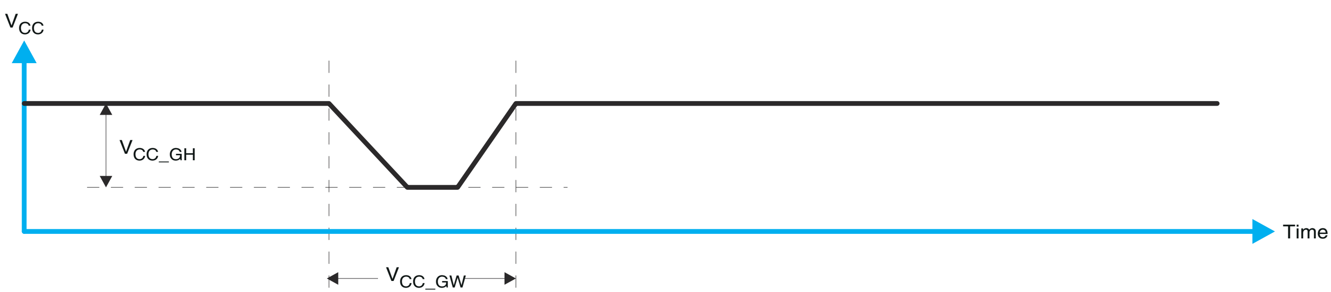

図 9-6. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to the default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 9-7 and 表 9-1 provide more details on this specification.

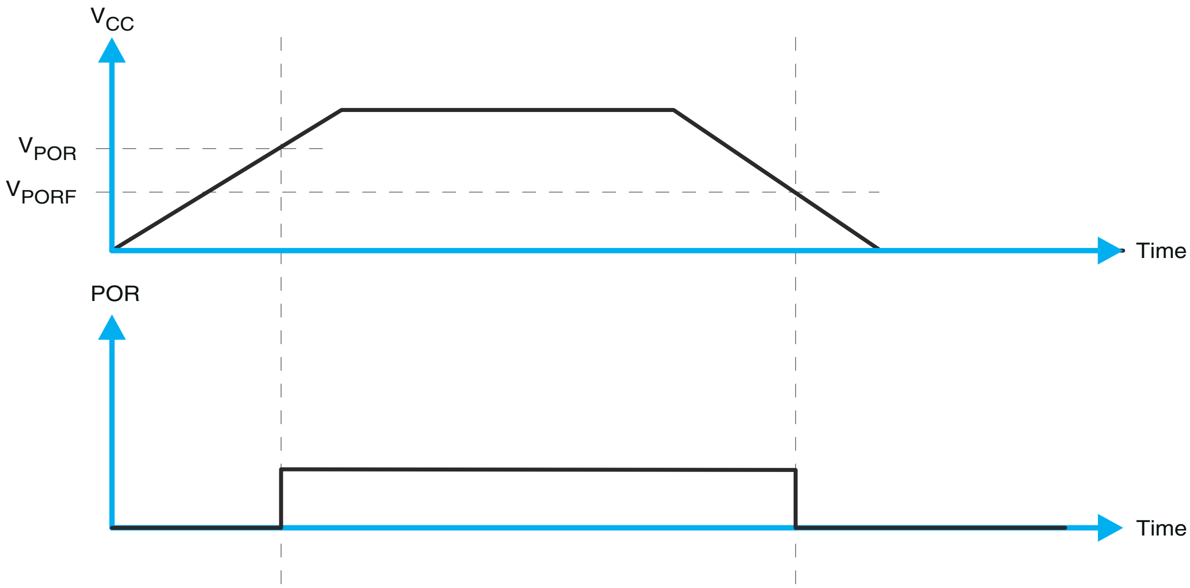

図 9-7. V_{POR}

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA6424ARGJR	ACTIVE	UQFN	RGJ	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PH424A	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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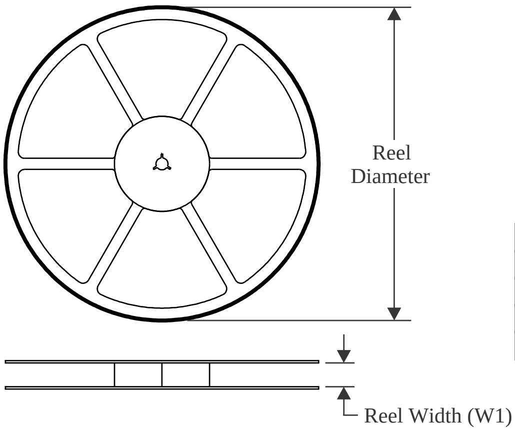
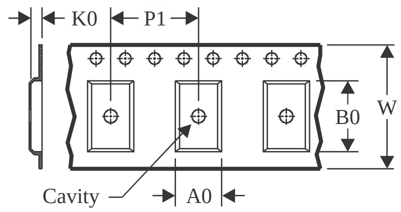
TAPE AND REEL INFORMATION

REEL DIMENSIONS

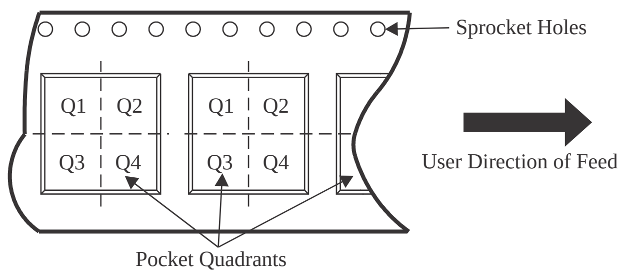


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

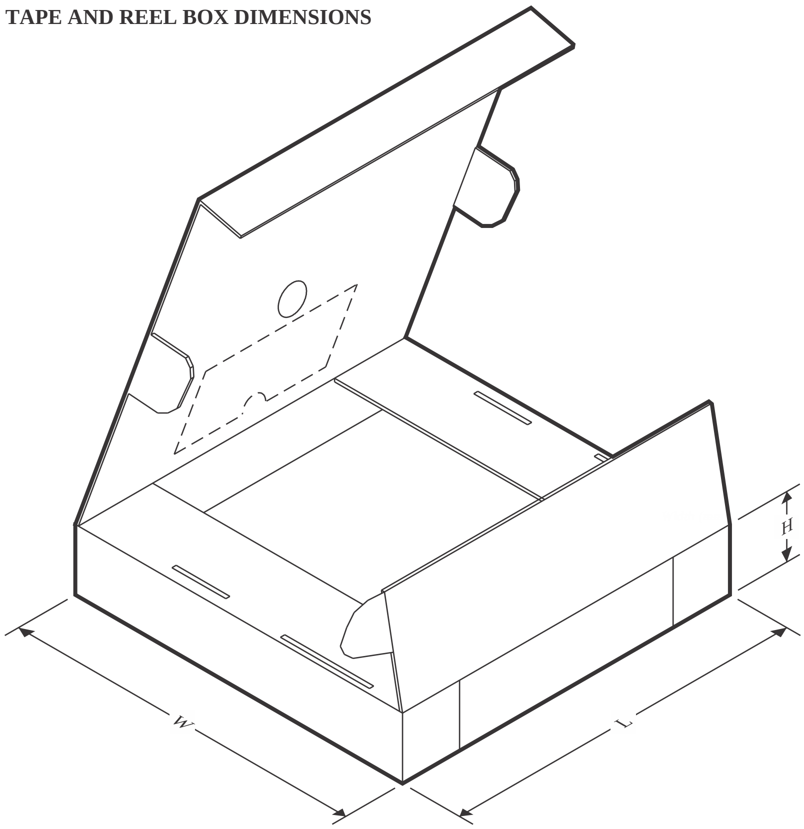
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

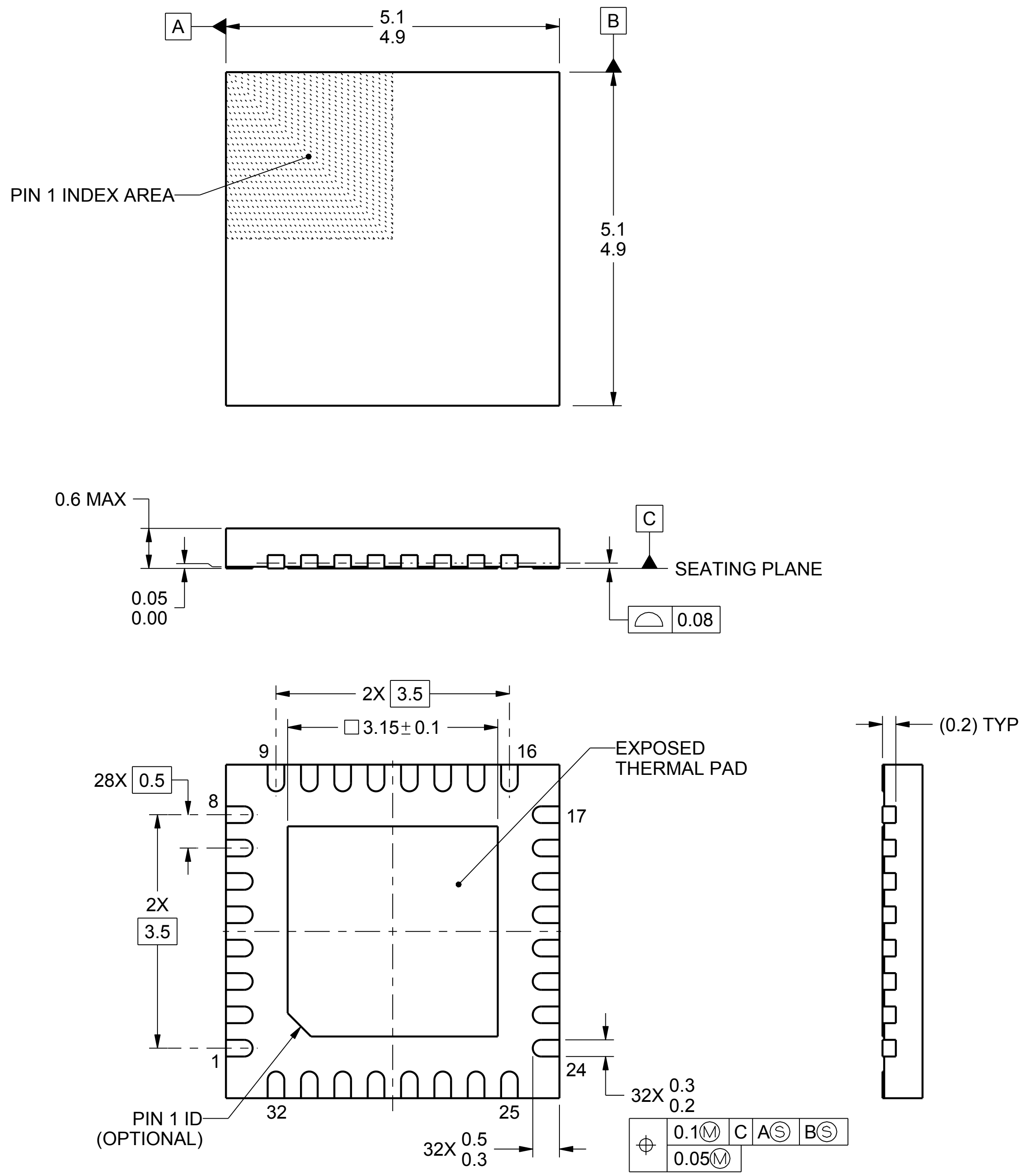
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA6424ARGJR	UQFN	RGJ	32	3000	330.0	12.4	5.3	5.3	0.75	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA6424ARGJR	UQFN	RGJ	32	3000	346.0	346.0	35.0



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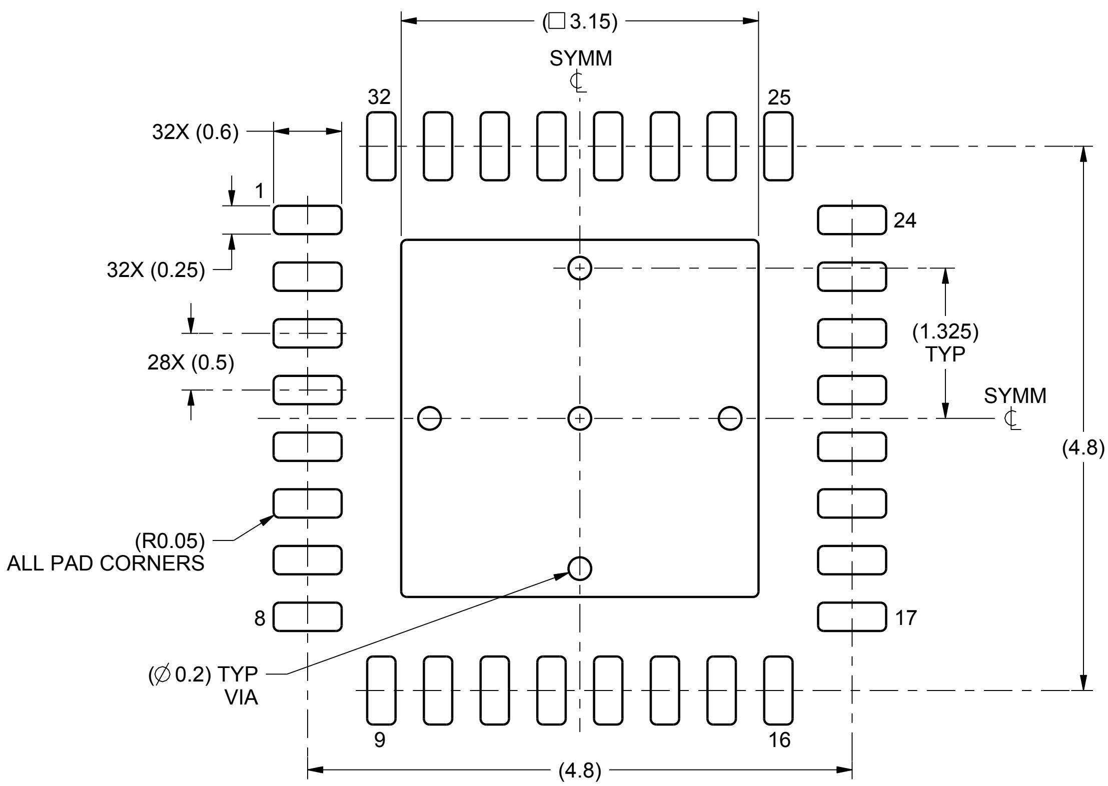
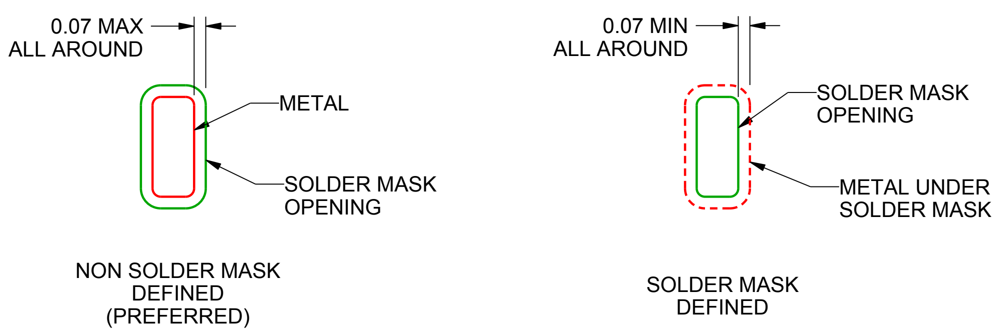
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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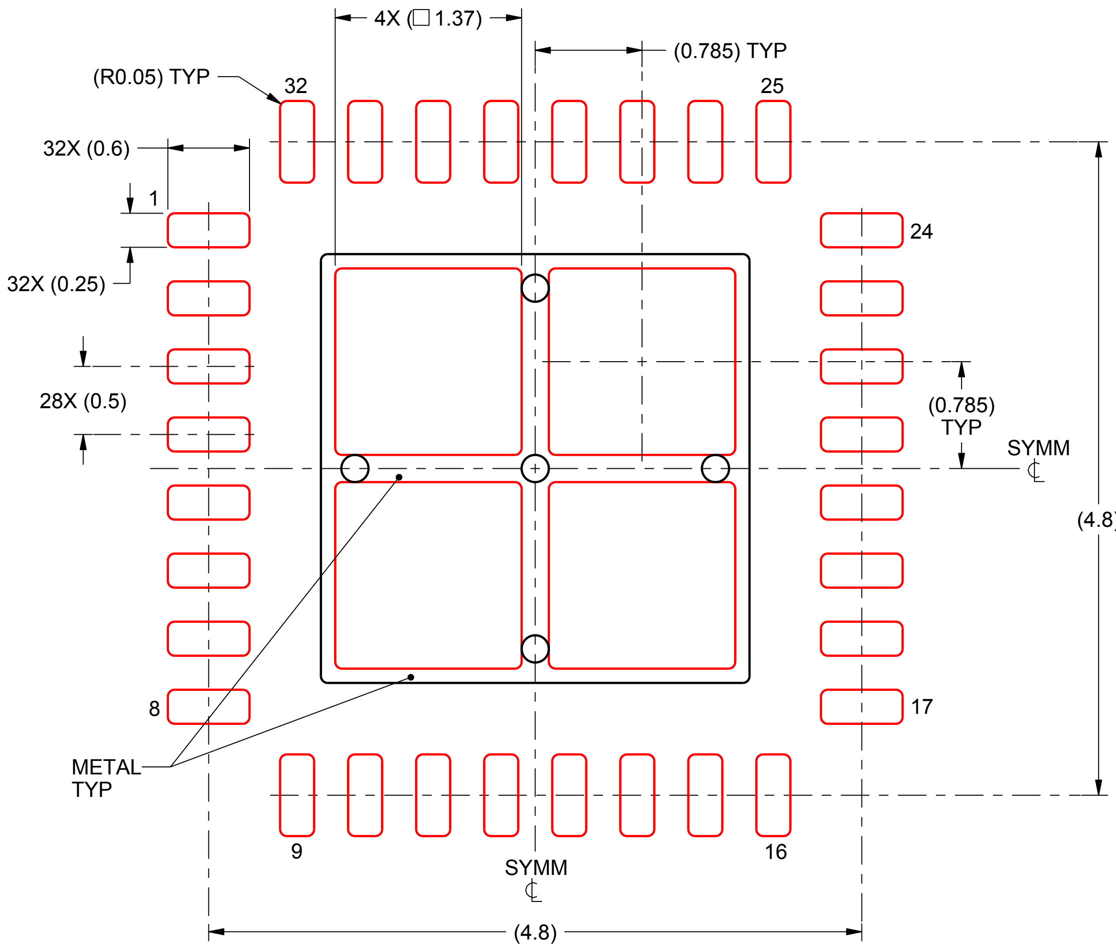
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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